1. Static RAM

1.1 Static RAM Memory Cell

A memory cell used in Hitachi static RAM consists of 4 NMOS transistors and 2 load resistors as shown in Figure 1-1. The data in the cell can be retained as long as power is supplied, and read out without being destroyed.

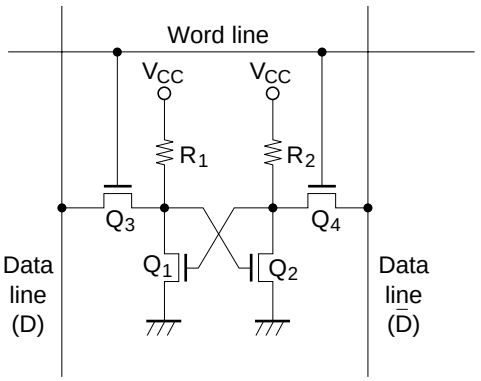


Figure 1-1 Static RAM Memory Cell

1.2 Data Retention Mode and Battery Backup System

The data in RAM is destroyed at power off. However, CMOS static RAM has a data retention mode. In this mode, power consumption at standby is extremely low and supply voltage can be reduced to 2 V. This enables a battery backup system to retain the data during power failure.

Data Retention Mode: The important point in designing a battery backup system is the timing relationship between the memory power supply and the chip select signal during a change from the ordinal power source and battery power. If proper timing for the change is missed, memory data might be destroyed.

Figure 1-2 shows the timing for switching the power supply. The definitions for the technical terms related to the data retention mode are as follows.

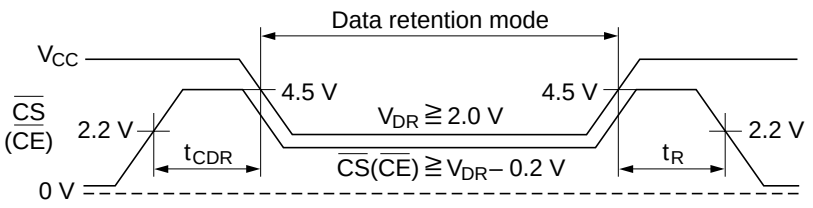


Figure 1-2 Timing for Battery Backup Application

Application

Data retention mode: The period during which the supply voltage is lower than the specified operation voltage. During this period, memory must be kept in non-select condition (e.g. $\overline{CS} \geq V_{DR}$ - 0.2 V).

t_{CDR} (time from chip select to data retention): The minimum time needed to change from operating mode to data retention mode. Normally 0 ns.

t_R (operation recovery time): The minimum time needed to change from data retention mode to operating mode.

V_{DR} (data retention voltage): The voltage applied in data retention mode. Normally the minimum supply voltage needed to retain memory data is 2 V.

I_{CCDR} (data retention current): The current consumption in the data retention mode depends on the memory power supply voltage and ambient temperature. It is specified as supply voltage, V_{DR} = 3.0 V.

Battery Backup System: The sequence of activities required to switch to battery backup is as follows.

1. External circuit detects a failure in the system power supply.
2. External circuit switches the RAM to standby mode.
3. External circuit separates the RAM from the system power supply.
4. External circuit switches to the backup power supply.

The control circuit detects the power failure and disconnects the power source after switching memory to the standby mode. On recovery, it confirms the power supply availability and, after some delay, returns memory to the operating mode. Memory control signals depend on the types of memory used in the system.

1. Using memory with only one $\overline{CS}$:

   The NAND signal between the control signal and chip select signal should be connected to $\overline{CS}$. Since the level of $\overline{CS}$ in the data retention mode must be higher than V_{DR} - 0.2 V, the power supply for this NAND gate must either be shared with the memory power supply or be pulled up to the memory power supply.
2. Using memory with two $\overline{CS}$:

   Basically, the signals are the same as above. In general use, two pins should be used for the control signal and the chip select signal, respectively. When the $\overline{CS}$ intercepts the current path of other pins in the input buffers, it is used as control signal input for the data retention mode.
3. Using memory with $\overline{CS}$ and CS:

   Since CS selects the chips at high level, it is preferable to use CS rather than $\overline{CS}$ as a control signal input for the data retention mode. As soon as power down is detected, the signals should be brought low. Therefore, a pull-up to the memory power supply level is not needed, thus simplifying the circuit organization.

Figure 1-4 shows an example of a battery backup system circuit. Hitachi recommends using CMOS logic for gate G1 in a control circuit and memory V_{CC}. The low V_{CE} transistor Q_1 is required to switch the regulating circuit from system power supply to backup power supply.

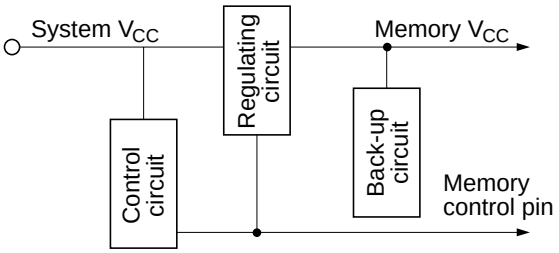


Figure 1-3 Example of Battery Backup System

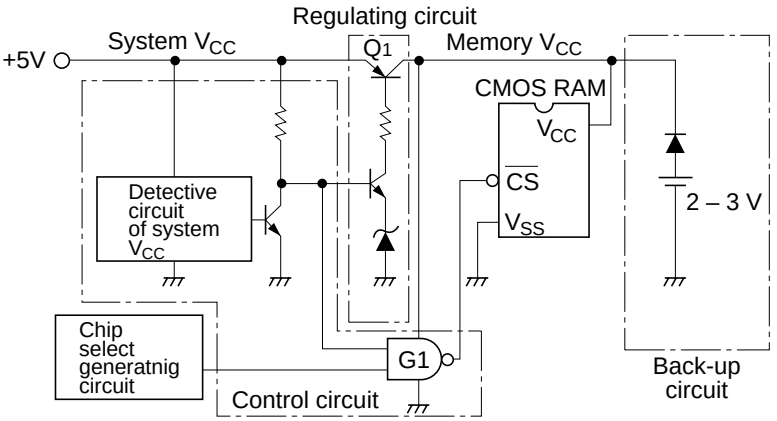


Figure 1-4 Example of a Battery Backup System Circuit

2. Pseudo-Static RAM

2.1 Pseudo-Static RAM Features

PSRAM is a new type of IC memory designed to meet the demands for lower power consumption and lower cost.

RAMs (random access memory) are roughly classified into DRAMs (dynamic RAM) and SRAMs (static RAM). These memories vary in characteristics such as density, cost, and control method because of differences of their memory cell structures. By understanding the advantages and disadvantages of each device, a system designer can choose the best product for his application.

The advantages of DRAM are high density and low cost. These features are a result of the simple and small structure of its memory cell, which consists of one transistor and one capacitor. However, DRAM requires refresh (periodic charging) along with external control signals for refresh. In addition, the address multiplex method of decreasing the number of pins to obtain high density requires external circuits, such as an address multiplexer for generating addresses in a time-shared manner. Thus, a system timing design using DRAMs becomes complicated.

Application

SRAM, on the other hand, does not require refresh and uses a non-address multiplex approach. Thus, SRAM can be interfaced to the MPU easily while keeping its external circuitry simple. However, SRAM requires a larger cell area and has lower density than DRAM because its memory cell is organized with 4 transistors and 2 resistors based on flip-flop circuits.

PSRAM has been developed as a new type of RAM providing the low cost per bit of DRAM and easy usage of SRAM. PSRAM offers the simple look of SRAM by providing part of the external circuits necessary with DRAM.

Table 2-1 lists the features of PSRAM, DRAM, and SRAM. PSRAM requires refresh like DRAM. One of three PSRAM refresh modes can be selected to match its system: address refresh, automatic refresh, and self refresh.

Figure 2-1 shows a comparison between systems using PSRAM and DRAM. By using PSRAM, many of the external circuits necessary for interfacing the MPU with DRAM can be eliminated.

Figure 2-2 shows a Block diagram of PSRAM.

Table2-1 Comparison of SRAM, PSRAM , AND DRAM Features

	SRAM	PSRAM	DRAM
Memory cell	4 transistors and 2 resistors	1 transistor and 1 capacitor	1 transistor and 1 capacitor
Density (same manufacturing process)	1 Mbits	4 Mbits	4 Mbits
Address	Non-address multiplex	Non-address multiplex	Address multiplex
Refresh	Not necessary	Necessary	Necessary
External circuit	Simple ⟵⟶		Complexed

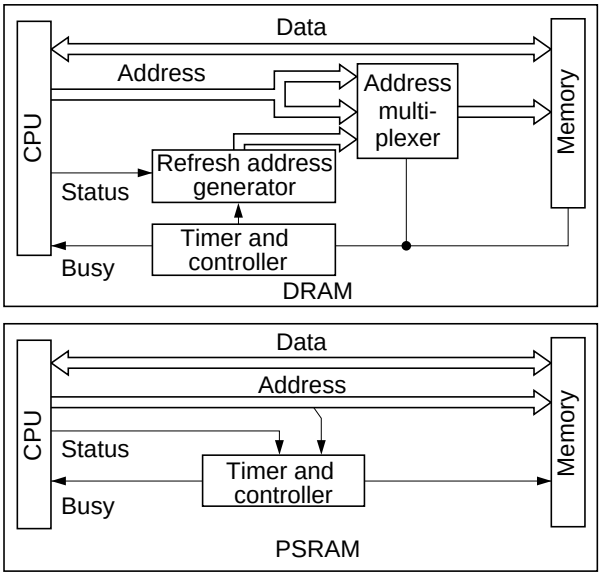


Figure 2-1 System Organization of DRAM and PSRAM

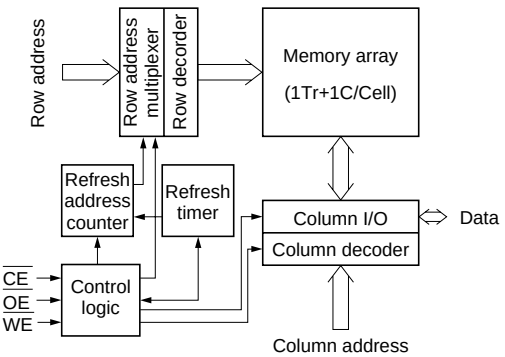


Figure 2-2 Block diagram of PSRAM

2.2 Pseudo-Static RAM Data Retention

PSRAM is useful in relatively small systems. Small systems require low current consumption since they often retain data with batteries. PSRAM with self-refresh retains data by internal refresh operation. Table 2-2 shows data retention characteristics.

Power supply voltage of data retention of PSRAM are different from that of SRAM. This is due to the use of different memory cell types. PSRAM uses an one-transistor type memory cell as used in DRAM. Refresh is internally done in order to retain data. This refresh operation is almost same operation as normal read/write, and it determines the low limit of the supply voltage. Though power supply voltage of standard PSRAM is 4.5 V - 5.5 V, some special parts retain data to 3.0 V. Please check the low limit of power supply in each data sheet.

2.3 Operation of 4M PSRAM HM658512A

The operation of HM658512A is explained here for understanding of PSRAM function.

2.3.1 Read/Write Cycle

Figure 2-3 and figure 2-4 show the timing chart for the read and write cycle of the HM658512A. The HM658512A can execute 2 types of accesses in the read cycle, a $\overline{CE}$ access (figure 2-3a) and an $\overline{OE}$ access (figure 2-3b). It writes data at the rising edge of $\overline{WE}$ (figure 2-4a) or at the rising edge of $\overline{CE}$ (figure 2-4b).

2.3.2 Refresh Cycle

Address refresh: This mode refreshes data by inputting row addresses 0-2047 through pins A0-A10 in sequence every 32 ms. Figure 2-5 shows the timing chart of distributed refresh.

Automatic refresh: This mode refreshes data with an internal refresh address which is generated by setting $\overline{OE}$/RFSH low with $\overline{CE}$ high. It is not required to input a refresh address from address pins since it is generated internally. Figure 2-6 shows the timing chart for distributed automatic refresh.

Self refresh: This mode refreshes data automatically at fixed periods with the internal refresh timer. The self refresh mode is enabled by keeping $\overline{OE}$/$\overline{RFSH}$ low for more than 8 µs with $\overline{CE}$ high. This mode reduces the number of external circuits necessary for refresh since both refresh addresses and refresh request signals are generated internally. Figure 2-7 shows the timing chart for self refresh. The width of the $\overline{OE}$/$\overline{RFSH}$ pulse while $\overline{CE}$ is high determines whether automatic refresh or self refresh is performed. When the pulse width exceeds 8 µs, the PSRAM enters self refresh mode. Self refresh mode is useful when retaining RAM data with batteries.

Table2-2 Data Retention of SRAM, PSRAM , AND DRAM

	SRAM	PSRAM	DRAM
Density (same manufacturing process)	1 Mbits	4 Mbits	4 Mbits
Data retention voltage	2 V to 5.5 V	4.5 V to 5.5 V[*1]	4.5 V to 5.5 V
Current consumption (when saving data)	1 µA (typ)	70 µA (typ)[*2]	150 µA (typ)[*2]
Refresh	Not necessary	Necessary (internal control)	Necessary (internal control)

Notes: 1. Some of PSRAMs retain data at 3.0 V.
2. Including refresh current. The typical values of HM658512A and HM51S4800C.

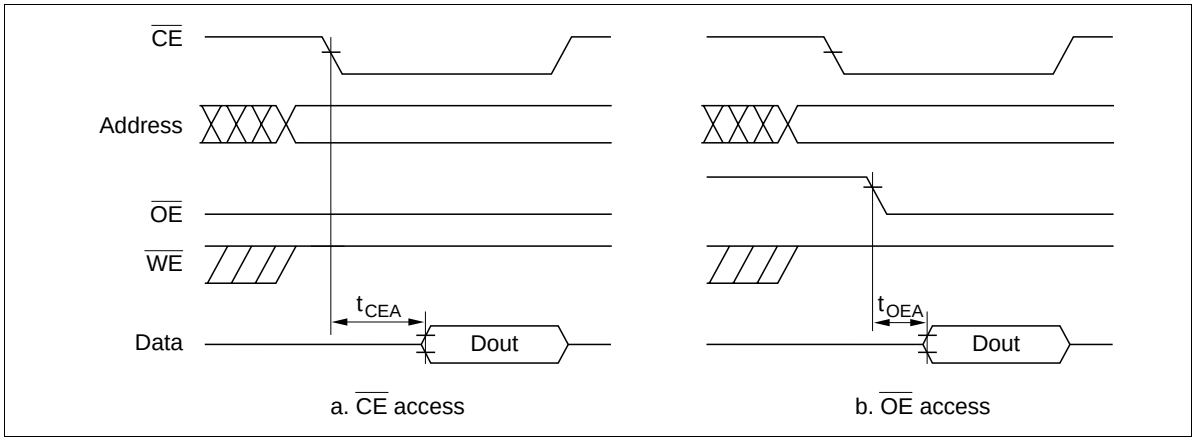


Figure 2-3 Read Cycle

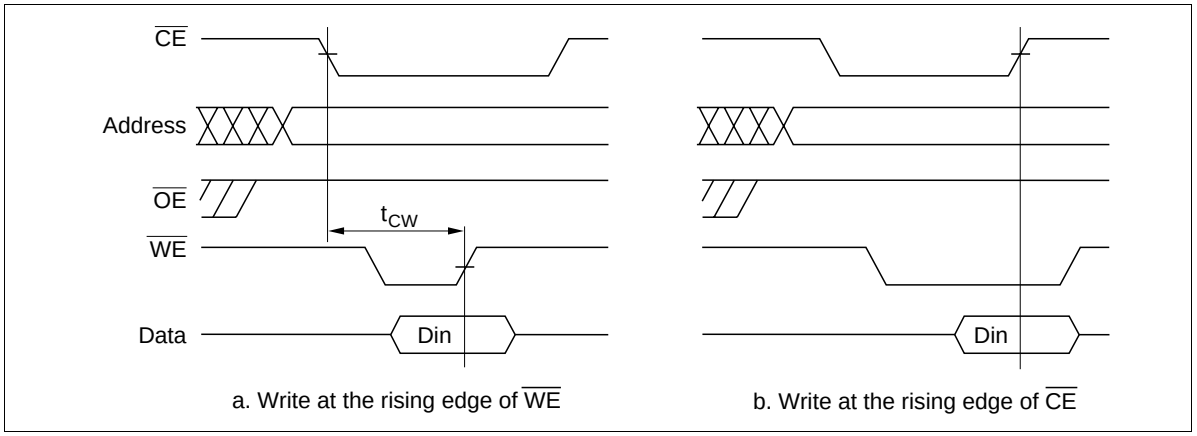


Figure 2-4 Write Cycle

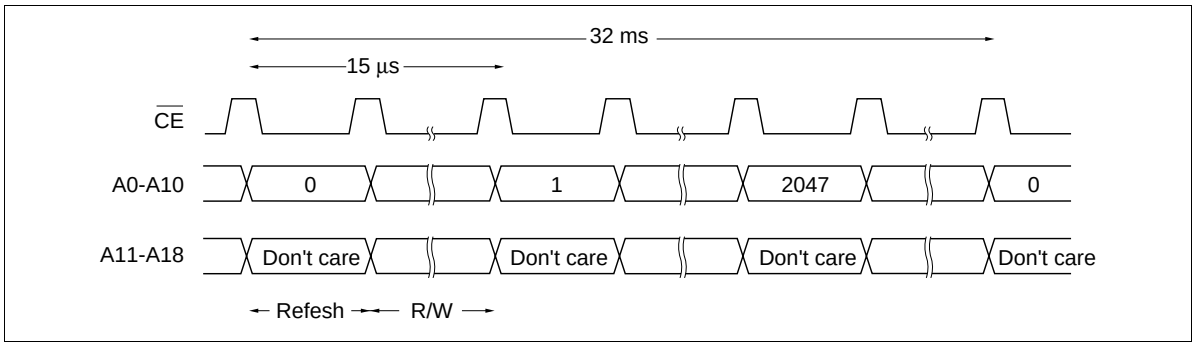


Figure 2-5 Address Refresh

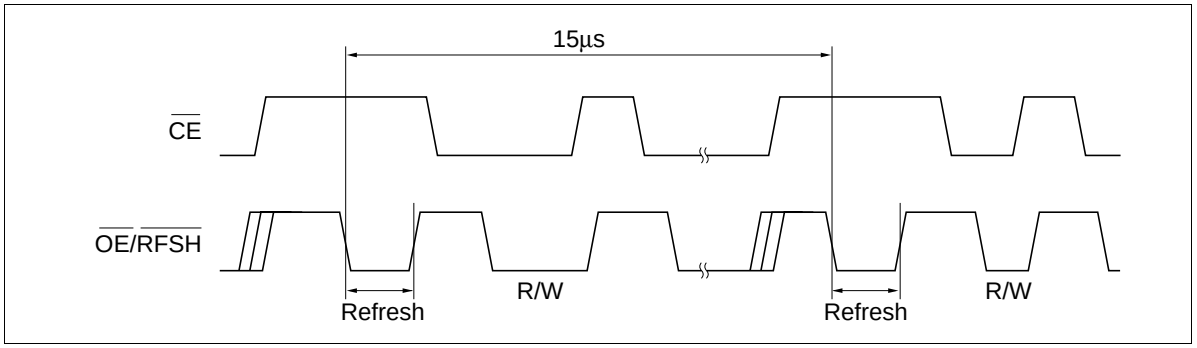


Figure 2-6 Automatic Refresh

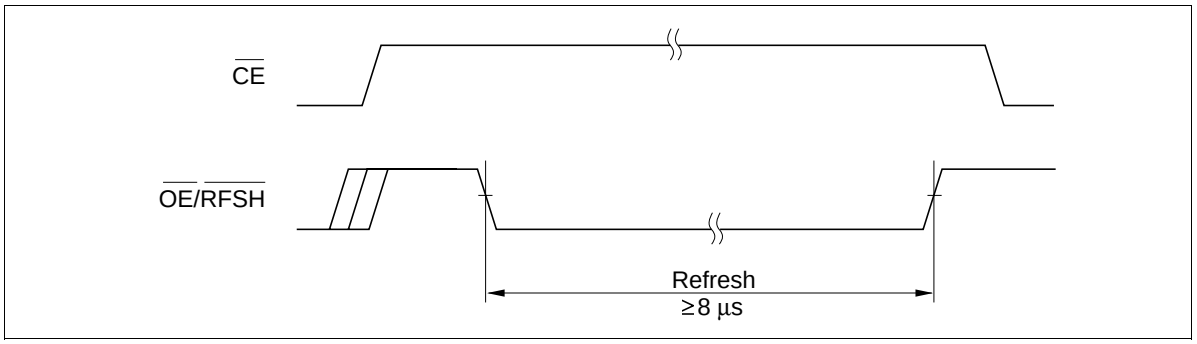


Figure 2-7 Self Refresh

2.3.3 Switching from Self Refresh Mode to Read/Write Mode

- After a self refresh is completed, the specification for t_{RFS} must be followed. t_{RFS} is defined as the time from a $\overline{OE}/\overline{RFSH}$ rising edge to the $\overline{CE}$ falling edge in the next cycle (see figure 2-8).
- When using address refresh cycles in read/write cycles, an address refresh must be started within 15 µs of completion of a self refresh, and the specified number of refresh cycles in the data sheet must be executed in succession.
- When using distributed automatic refresh cycles in read/write cycles, the first cycle of a distributed refresh must be executed within 15 µs of completion of a refresh.

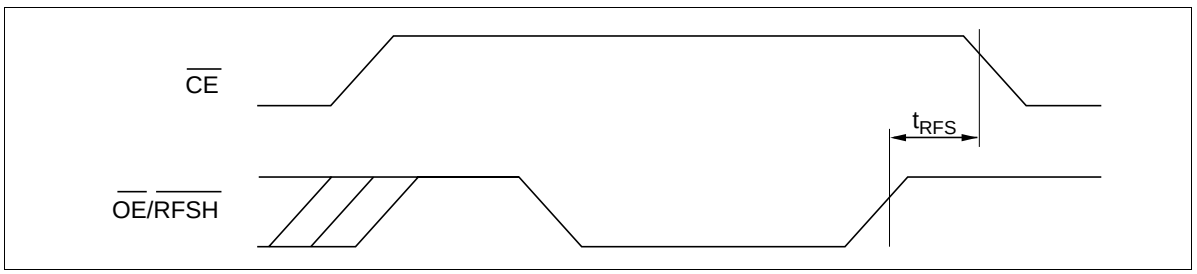


Figure 2-8 t_{RFS} (Refresh Rest Time)

- When using burst automatic refresh cycles in read/write cycles, the first cycle of automatic refresh must be started within 15 µs of completion of self refresh, and the specified number of refresh cycles in the data sheet must be executed in succession.

2.3.4 Initialization

Hitachi's PSRAM can start operation by executing eight or more initialization cycles (dummy cycles) at least 100 µs after the power voltage reaches 4.5 V - 5.5 V after power-on. An automatic refresh cycle can be used for initialization, where one automatic refresh cycle is equivalent to one initialization cycle.

2.3.5 Miscellaneous Notes

- If a short $\overline{CE}$ pulse of a width less than t_{CE} min is applied to RAM, an incomplete read occurs and stored data may be destroyed. Make sure that $\overline{CE}$ low pulses of less than t_{CE} min are inhibited. Note that a 10-ns $\overline{CE}$ low pulse may sometimes occur owing to the gate delay on the board if the $\overline{CE}$ signal is generated by the decoding of higher address signals on the board. Avoid these short pulses. One way to this $\overline{CE}$ short pulse is by gating the decoded addresses with an address strobe input.
- $\overline{OE}/\overline{RFSH}$ works as refresh control in standby mode. A short $\overline{OE}/\overline{RFSH}$ low pulse in standby mode may cause an incomplete refresh that will destroy data. Make sure that $\overline{OE}/\overline{RFSH}$ low pulse of less than t_{FAP} min are also inhibited. The definitions of t_{CE} and t_{FAP} are shown in the pages of HM658512A.
- PSRAM is more sensitive to noise than normal SRAM since it executes dynamic operation internally like DRAM. It is recommended to insert one bypass condenser per RAM.
- The $\overline{OE}/\overline{RFSH}$ pin has two functions, $\overline{OE}$ for output enable and $\overline{RFSH}$ for refresh control. The specifications for parameters such as t_{OHC} and t_{OCD} must be followed to distinguish $\overline{OE}$ and $\overline{RFSH}$.

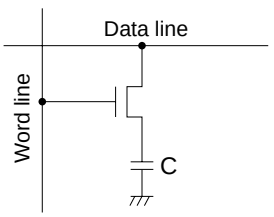


Figure 2-9 Memory cell of PSRAM

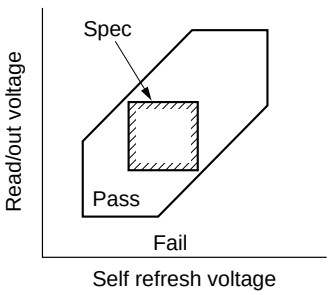


Figure 2-10 Data reteintion voltage

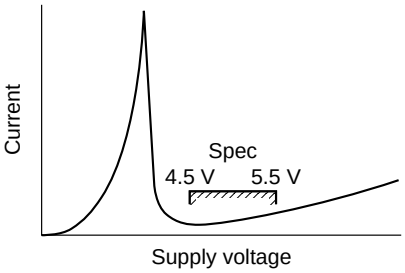


Figure 2-11 Supply voltage and self refresh current

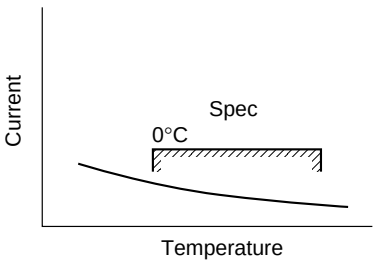


Figure 2-12 Temperature and self refresh current

3. Instructions for Using Memory Devices

3.1 Prevention of Electrostatic Discharge

As semiconductor memory designs are based on a very fine pattern, they can be subject to malfunction or defects caused by static electricity. Though the built-in protection circuits assure unaffected reliability in normal use, devices should be handled with these precautions:

1. In transporting and storing memory devices, place them in a conductive magazine or wrapper, or put all pins of each device into a conductive mat, so that they are kept at the same potential. Manufacturers should give sufficient consideration on proper packing when shipping their products.
2. When the devices are to be touched during mounting or inspection, the handler must be grounded. Do not forget to connect a resistor (1 MΩ approximately is desirable) in series for protect 10 n against electrical shock.
3. Keep the relative ambient humidity at about 50% during processing.
4. For working clothes, cotton is preferable to synthetic fabrics.
5. Use a soldering iron operating at low voltage (12 V or 24 V, if possible) with its tip grounded.
6. When transporting a board with memory devices mounted on it, enclose it with conductive materials.
7. Use conductive materials of high resistance (about 10^9 ohms) to protect the devices from electrostatic discharge. Otherwise, if accident-ally put in contact with conductive materials such as a metal sheet, the devices may deteriorate or even breakdown, owing to the sudden release of charge stored on the surface.

8. Never set a system in which memory devices are used near anything that generates high voltage (e.g., a CRT anode electrode, etc.).

3.2 Using CMOS Memories

As shown in Figure 3-1, the input of a CMOS memory is connected to the gate of an inverter consisting of PMOS and NMOS transistors. Figure 3-2 shows the relationship between the input voltage and current within the inverter. The top and bottom transistors turn on and create a current flow when the input voltage reaches an intermediate level. Therefore it is necessary to keep the input voltage below 0.2 V or above V_{CC} - 0.2 V in order to minimize power consumption. The data sheet specifies the standby current for two cases of input level (with minimum V_{IH} and maximum V_{IL}, and with 0.2 V or V_{CC} - 0.2 V), and the difference in values as being remarkably great. Some memory devices are designed to cut off such current flow in the standby mode by the control of input signals, but this depends on the specific device type. This should be confirmed in data sheets for each device type.

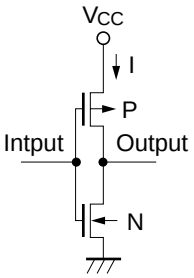


Figure 3-1 CMOS Inverter

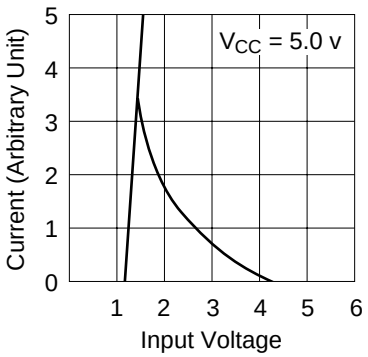


Figure 3-2 Relationship Between Input Voltage and Current in a CMOS Inverter

Application

Another problem peculiar to CMOS devices is latch up. Figure 3-3 shows the cross section of a CMOS inverter and the structure of a parasitic bipolar transistor. The equivalent circuit of the parasitic thyristor is shown in Figure 3-4. When positive DC current or pulse noise is applied (Figure 3-4a), T_{R3} is turned on owing to the bias voltage generated between the base and emitter. Also, trigger current flows to ground through R_P, the base resistance of T_{R2}. As a result, T_{R2} becomes conductive and the current flows from power supply (V_{CC}) through the base resistance of T_{R1} (R_N), which also puts T_{R1} into conduction. Then as the base of T_{R2} is rebiased by the collector current from T_{R1}, the closed loop consisting of T_{R1} and T_{R2} reacts. Thus, current flows constantly between the power supply (V_{CC}) and ground even without the trigger current caused by outside noise.

Latch up can also be caused by a negative pulse (Figure 3-4b). Most semiconductor memory manufacturers are trying to improve latch up immunity in their products. Hitachi provides a broad enough guard band by applying a diffusion layer around the inputs and outputs, taking care not to connect the input to the p^+ diffusion layer. The input voltage for the 64-kbit static RAM HM62256, for example, is specified as follows:

V_{IH} max 6.0 V (not dependent on V_{CC})
V_{IL} min 3.0 V (pulse width = 50 ns)
-0.5 V (DC level)

Thus almost no consideration for latch up is required in system designs using these devices.

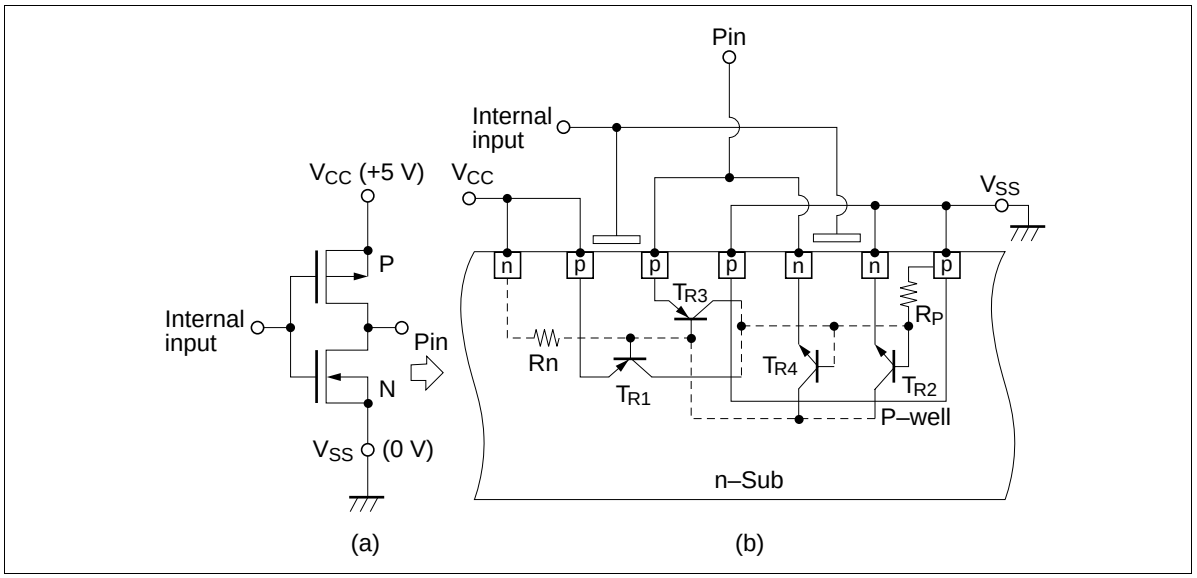


Figure 3-3 Cross Section Structure of CMOS Inverter

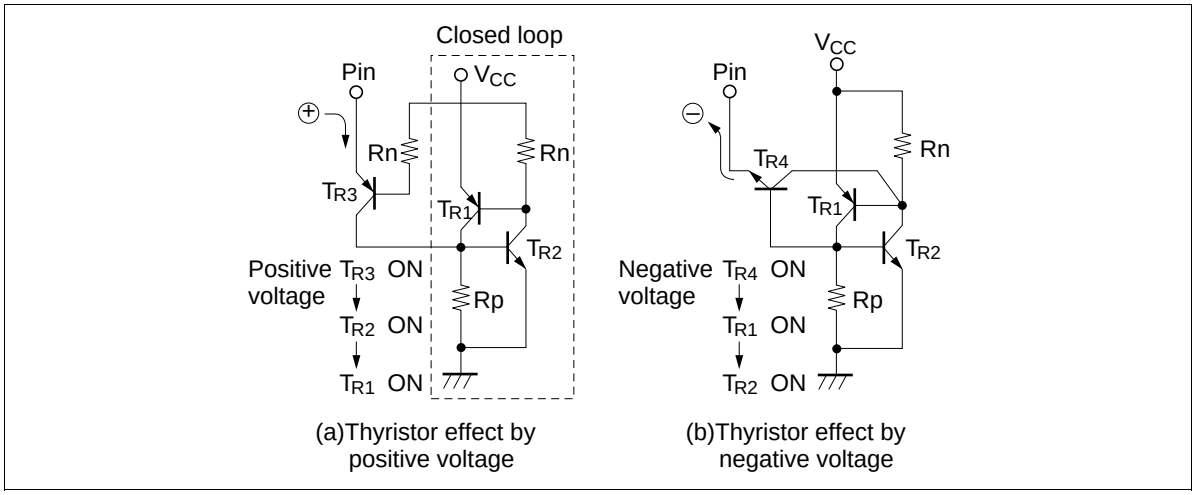


Figure 3-4 Equivalent Circuit of Parasitic Thyristor

3.3 Noise Prevention

Noise in semiconductor memories is roughly classified as input signal noise and power supply noise.

Input Signal Noise: Input signal noise is caused by overshoot and undershoot. If either of them exceeds the recommended DC operating conditions, normal operation is hindered, and a voltage over the absolute maximum rating will break the device. When operating high speed systems, special care is required to prevent input signal noise.

The noise can be prevented by inserting a serial resistance of less than 50 ohms into each input or a terminating resistance into the input line. Actually, however, input signal noise can be simply reduced by a stable power supply line, because the noise is often caused by an unstable reference voltage (ground level).

Power Supply Noise: Power supply noise can be classed as low-frequency and high-frequency as shown in Figure 3-5. To assure a stable memory operation, combined low- and high-frequency noise should be held below 10 percent of the standard level of the peak-to-peak power supply voltage.

Devices like dynamic RAMs, which operate from clock signals, or high speed CMOS static RAMs, through which current flows during the transition of signals, consume high peak current. When a power supply does not have enough capacity for the peak current, the voltage drops. And if the recovery rate of the power supply synchronizes with its time constant, it may start oscillating. To reduce the influence of the peak current, a bypass capacitor of 0.1-0.01 μF should be inserted near the device. The following points must be considered in designing the layout of a board:

1. For bypass capacitors, use titanium, ceramic, or tantalum capacitors which have better high-frequency characteristics.
2. Bypass capacitors must be applied to the power supply pins of memory devices as near as possible, and inductance in the path from the V_{CC} pin to V_{SS} pin through the bypass capacitor must be kept as low as possible.
3. The line connected to the power supply on the board should be as wide as possible.

4. It is preferable for the power supply line to be at right angles to devices selected at the same time, otherwise too much peak current will flow through one power supply line at a time.

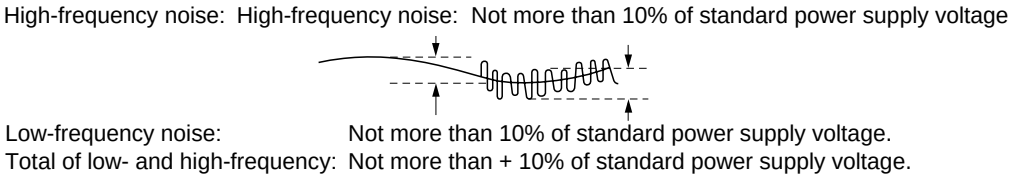


Figure 3-5 Power Supply Noise

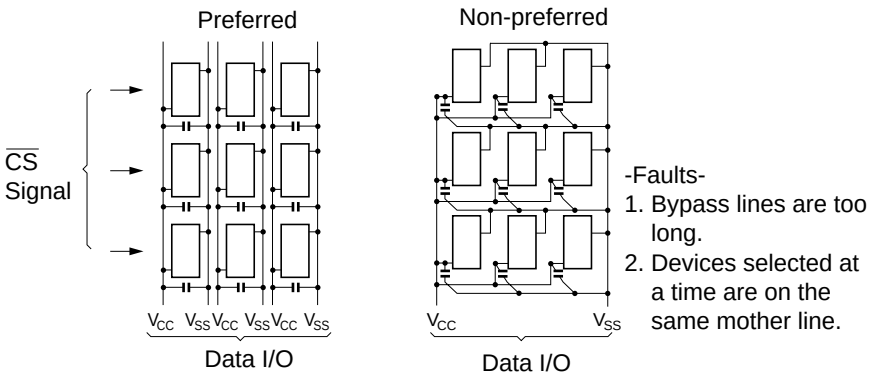


Figure 3-6 Examples of a Power Supply Board Pattern

1. Specific Memories for Graphic/Video Applications

1.1 Multiport Video RAM

Figure 1-1 shows the general concept of video RAM. A multiport video RAM provides an internal data register (SAM) with memory (RAM). Both can be accessed asynchronously. Effective graphic display memory can be developed by using the random port of the RAM component for graphic processor drawing, and the serial port of the SAM component for CRT display.

Figure 1-2 shows the block diagram of the 1-Mbit multiport video RAM HM534251B and HM538123B and Table 1-1 shows the operation modes of the HM534251B and HM538123B.

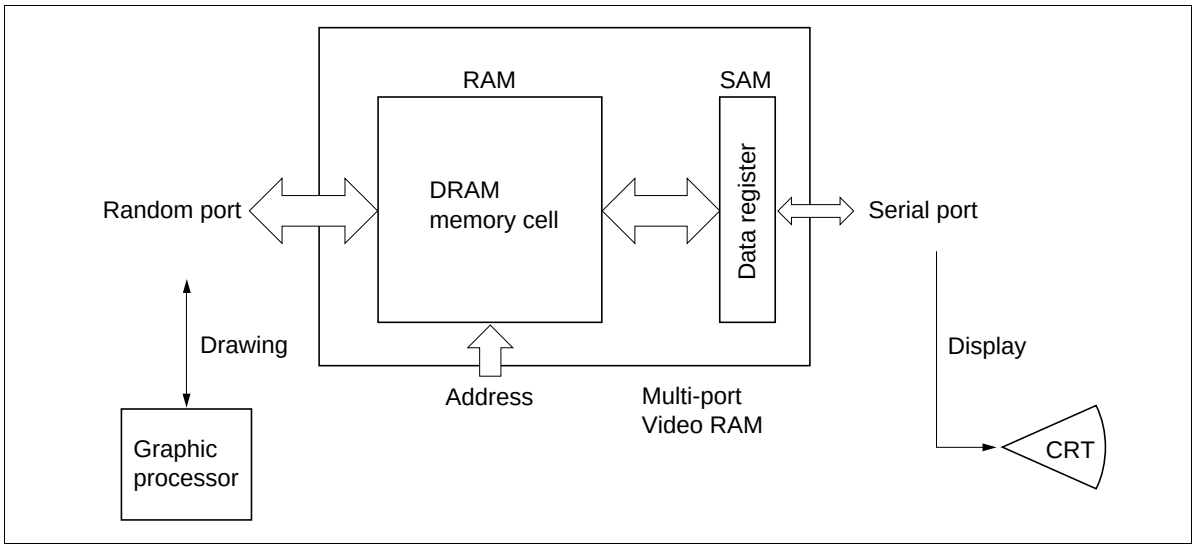


Figure 1-1 A General Concept of Multiport Video RAM

Application

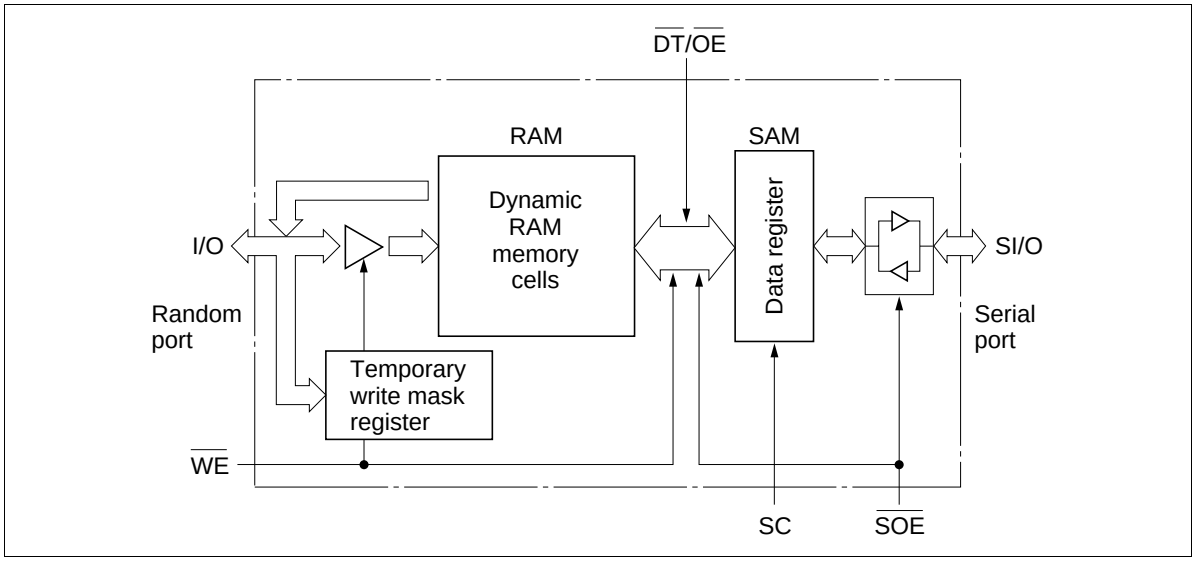


Figure 1-2 Block diagram of HM534251B and HM538123B

The operation modes shown in Table 1-1 are described as follows.

Read/Write Operation: Read/write is performed on the random port in the same sequence as a dynamic RAM (Figure 1-3). The HM534251B and HM538123B start the read operation with $\overline{WE}$ high and the write operation at the falling edge of $\overline{WE}$.

Table 1-1 Operation Modes of HM534251B and HM538123B

At the Falling Edge of $\overline{RAS}$					SAM Modes	
$\overline{CAS}$	$\overline{DT/OE}$	$\overline{WE}$	$\overline{SOE/SE}$	RAM Modes	SI/O Direction	Notes
H	H	H	X	Read/write	Sin/Sout	1, 2, 3
H	H	L	X	Temporary write mask data program	Sin/Sout	1, 2, 3
H	L	H	X	Read trandfer	Sout	2
H	L	L	L	Write transfer	Sin	
H	L	L	H	Pseudo transfer	Sin	
L	X	X	X	CBR refresh	Sin/Sout	1, 2

H: High, L: Low, X: Don't care

Notes: 1. The transfer cycle executed previously defines SI/O direction.
2. SI/O is in a high impedance state with $\overline{SOE}$ high, even of the direction is Sout.
3. The HM534251B and HM538123B start write opreation if $\overline{WE}$ is low at the falling edge of $\overline{CAS}$ or becomes low between the falling edge of $\overline{CAS}$ and the rising edge of $\overline{RAS}$.

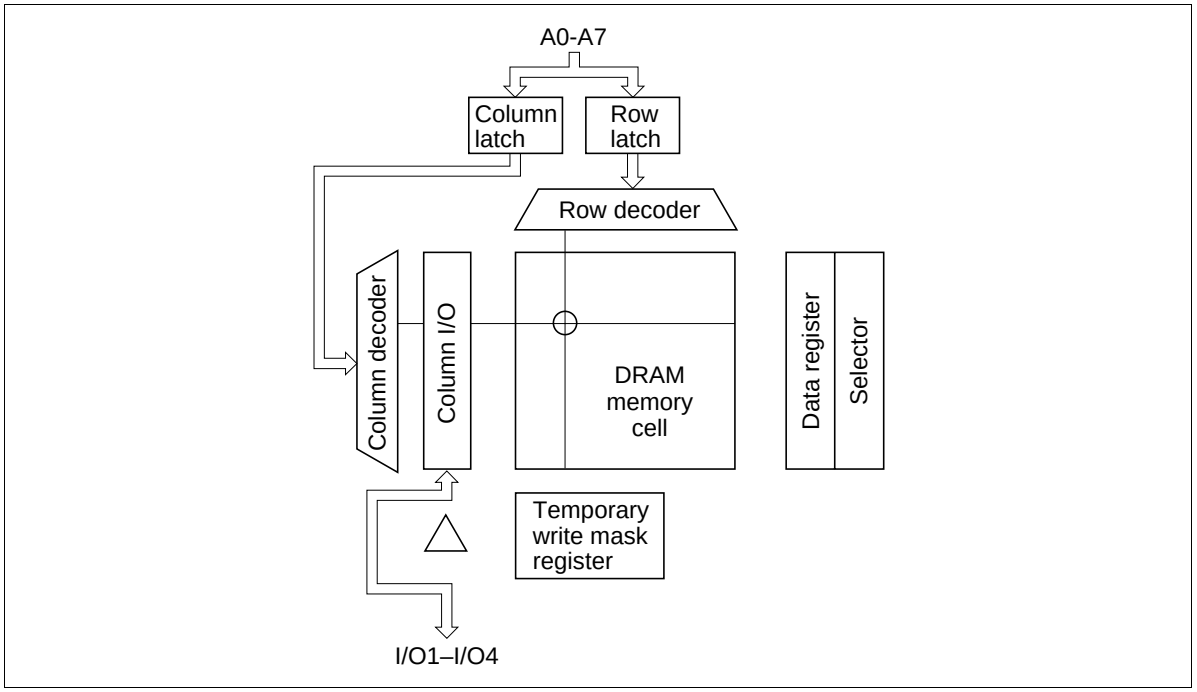


Figure 1-3 Read/write Operation

Temporary Write Mask Set and Temporary Masked Write Operation: The HM534251B and HM538123B provide a temporary masked write operation which inhibits writing data bit-by-bit (write mask) during one $\overline{RAS}$ cycle. The temporary write mask set function defines the bits to be inhibited (Figure 1-4). This operation puts the data on I/O1-I/O4 into the internal temporary write mask register. When 0 is programmed to the regist-er, writing to the corresponding bit is inhibited.

The temporary write mask register is reset at the rising edge of $\overline{RAS}$.

Read Transfer Operation: In this cycle, the HM534251B and HM538123B transfer the data of one row in RAM (1024 bits), at the address specified by the falling edge of $\overline{RAS}$, to SAM (Figure 1-5). The start address in SAM can be programmed at the falling edge of $\overline{CAS}$ in this cycle. After data transfer, the serial port is set to the serial read mode at the rising edge of $\overline{DT}/\overline{OE}$.

Write Transfer Operation: In this cycle, the HM534251B and HM538123B transfer the data in the SAM data register (1024 bits) to one row in RAM, at the address specified by the falling edge of $\overline{RAS}$ (Figure 1-6). The start address in SAM can be programmed in this cycle. After data transfer, the serial port is set to serial write mode.

Pseudo Transfer Operation: This operation switches the serial port to serial write mode (Figure 1-7). It does not perform data transfer between RAM and SAM. The SAM start address can be programmed in this cycle.

$\overline{CAS}$-before-$\overline{RAS}$ refresh operation: The HM534251B and HM538123B perform refresh by using the internal address counter in this operation (Figure 1-8).

Application

Serial read/write operation: The HM534251B and HM538123B read/write the contents of the SAM data register in serial mode at the rising edge of SC (serial clock input) (Figure 1-9). The address for serial access is generated by the internal address pointer, independent of the random port operation. It should be considered that serial access is restricted in transfer cycles. The SAM, employing static-type data registers, requires no refresh.

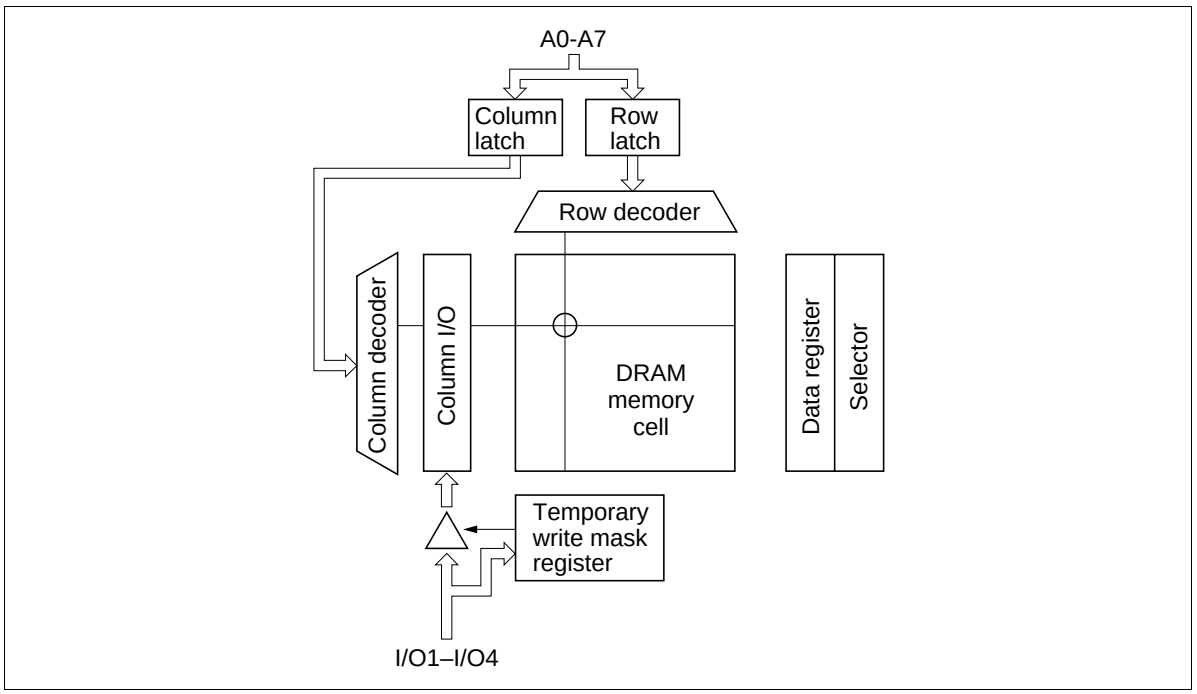


Figure 1-4 Tempotary Masked Write Operation

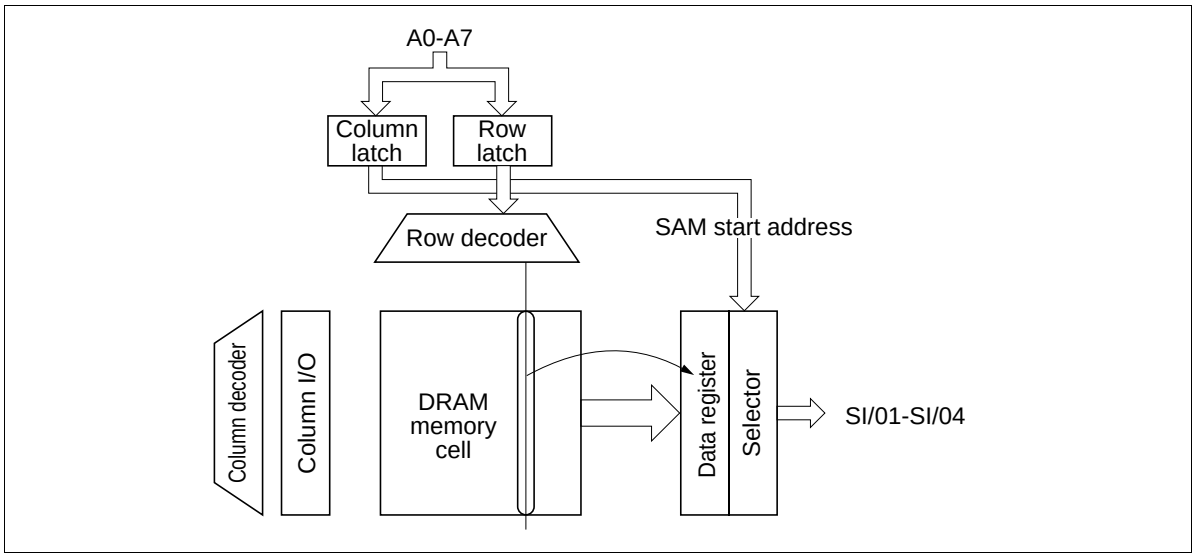


Figure 1-5 Read Transfer Operation

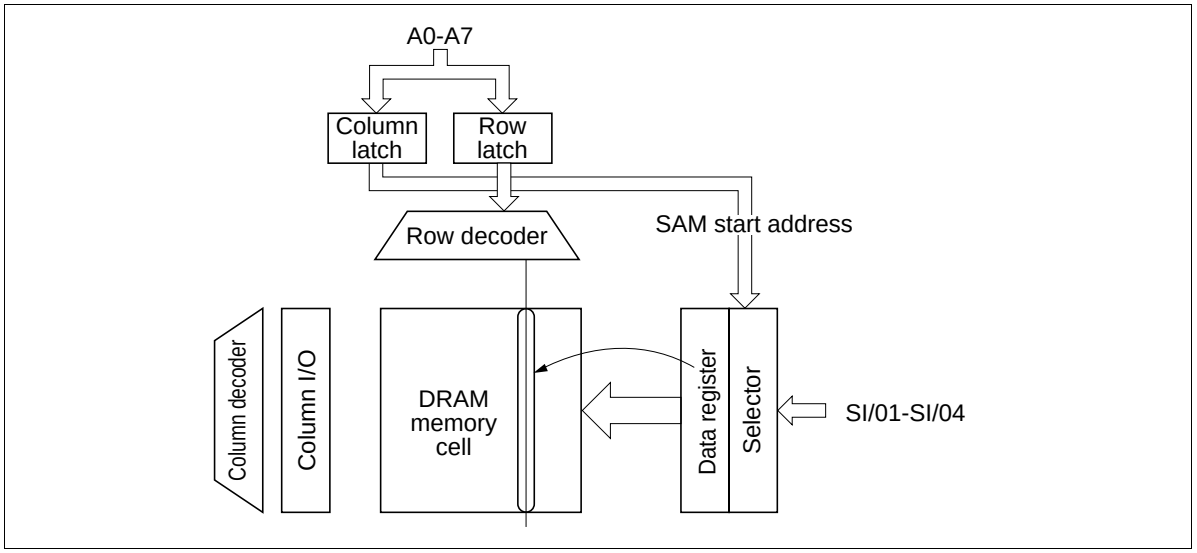


Figure 1-6 Write Transfer Operation

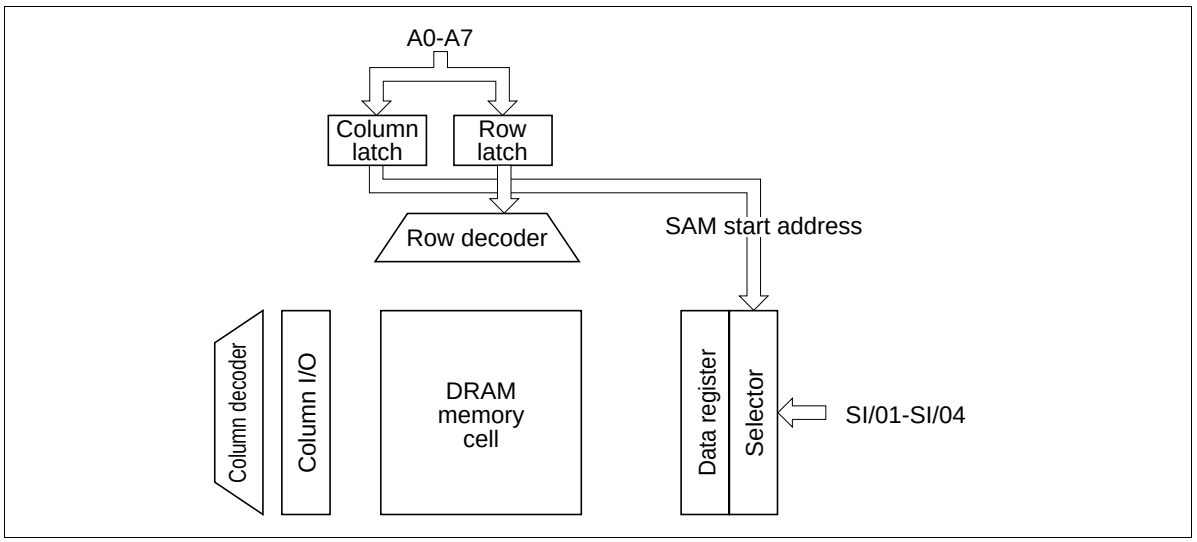


Figure 1-7 Pseudo Transfer Operation

Application

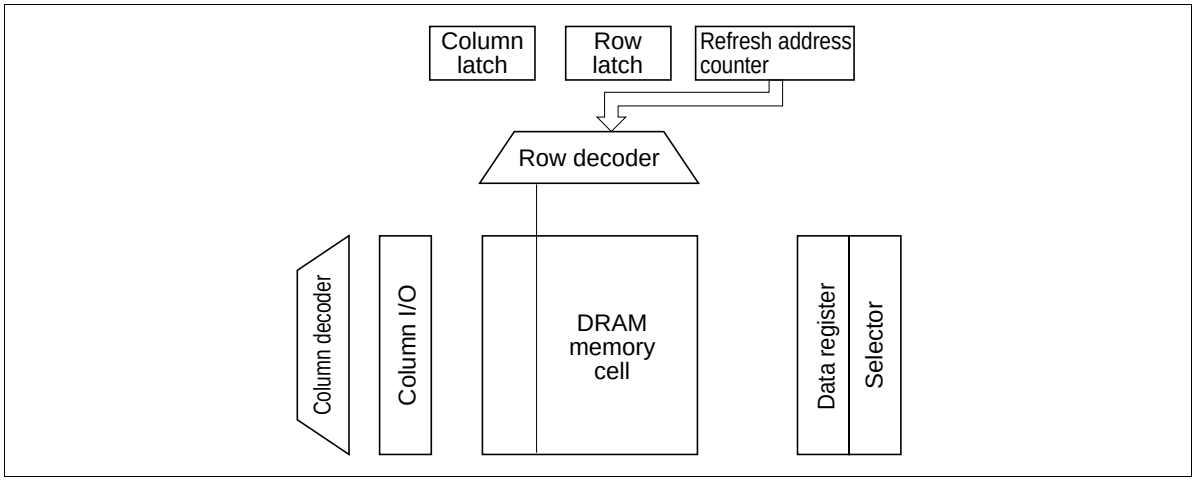


Figure 1-8 $\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh

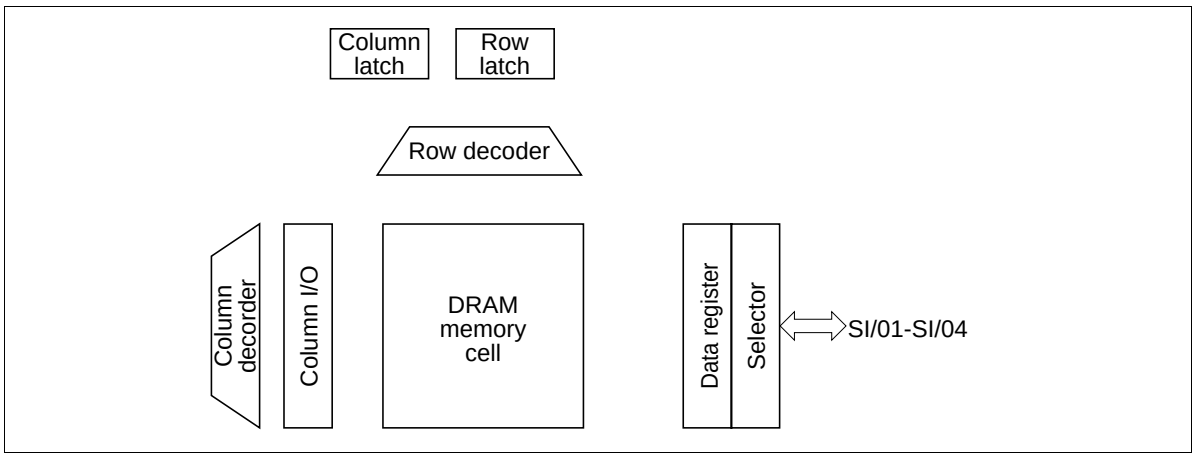


Figure 1-9 Serial Read/Write Operation

Notes: Notes on using HM534251B and HM538123B are as follows.

- Dummy $\overline{\text{RAS}}$ cycle

  Devices should be initialized by eight dummy $\overline{\text{RAS}}$ cycles (minimum) before accessing the random port. The refresh cycle can be inserted for initialization. It is recommended that the system be initialized by a dummy $\overline{\text{RAS}}$ cycle in the automatic reset time of the processor.

- Bypass capacitor

  One bypass capacitor should be inserted between V_{CC} and V_{SS} to each device. The V_{CC} pin should be connected to the capacitor by the shortest path. A capacitor of several μF is suitable.

- Negative voltage input

  A negative polarity input level to an input pin or I/O pin should be above -1 V. In this range, it has no effect on the device characteristics or RAM/SAM data retention.

2. Dynamic RAM (DRAM)

2.1 Features of DRAM

DRAM has a simple two-element memory structure, consisting of a single transistor and a single capacitor. Due to this feature, DRAM is suitable for a higher degree of chip integration and can implement low-price products, although they operate only at medium-range speeds. Therefore, DRAM is widely used as image memory, in addition to main memory in personal computers, workstations, and mainframe computers. DRAM requires a rewrite operation, called "refreshing," at a regular interval because information in memory cells is stored in the form of electric charges in capacitors.

2.2 Basic Operation of DRAM

Using the one-transistor cell method (Figure 2-1), the mainstream of today's DRAM memory cells, as an example, we explain the basic operation of one-transistor cells and discuss the basic read and write operations of DRAM, as shown in Figure 2-2.

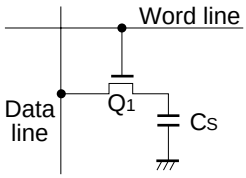


Figure 2-1 The One-Transistor Cell Method

Application

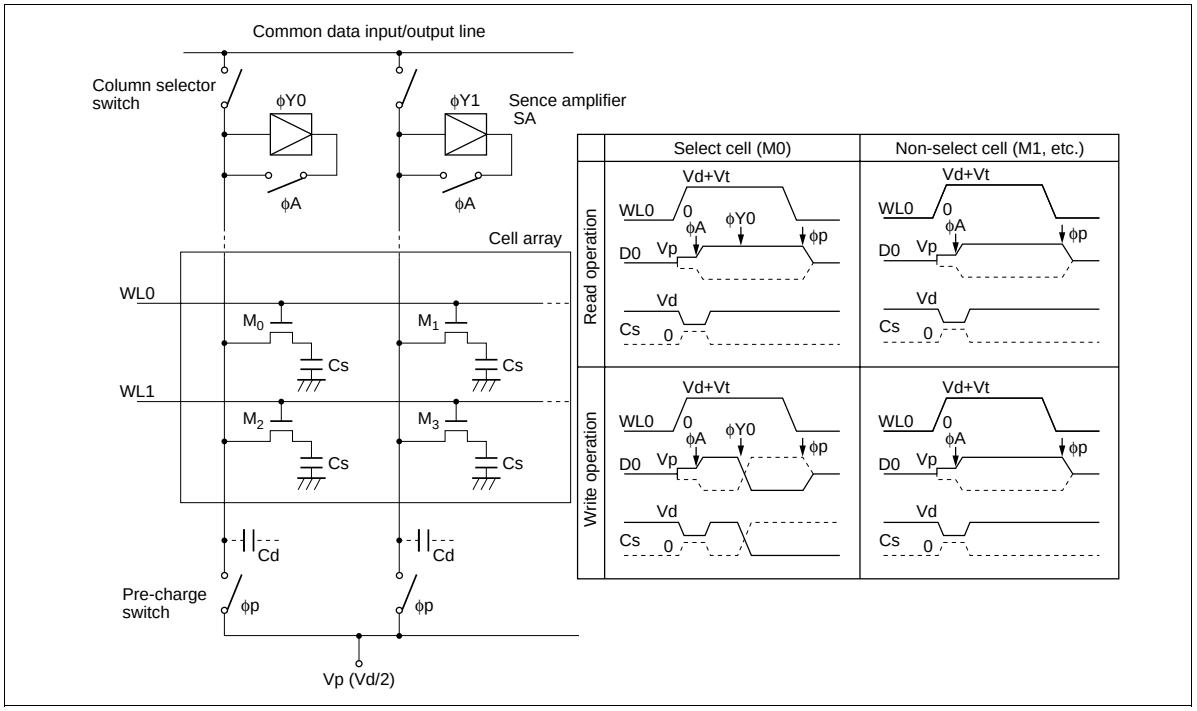


Figure 2-2 Basic Operation of One-Transistor Cells

(1) Pre-charge Operation

Before memory cells operate, they must be pre-charged so that the data line will be set at a certain voltage, called "pre-charge voltage" (Vp). Typically, the value of Vp is halfway between the high voltage (Vd), which is to be written into memory cells, and the low voltage (0). This is what is known as the Vd/2 pre-charging method. This method helps reduce power consumption and noise resulting from the charge and discharge operations of the data line.

(2) Read Operation

An operation that will read the memory cell (M0) of a certain property to be chosen proceeds as follows. First, the word line (WL0) to which M0 is connected is selected, and a pulse voltage is added to the word line. Then, the signal voltage (V_S) that changes with the information voltage (Vd, 0) of the capacitor CS in M0 is added to the pre-charge voltage. The resulting voltage appears in the positive/negative form of on the data line. The value of Vs is expressed by the following:

$V_S = Vd/2 * C_S/(C_S + Cd)$

The Cd is parasitic capacitance in the data line and it is by far greater than the value of CS. The sense amplifier (SA) on the data line senses and amplifies the low positive/negative signal voltage using the pre-charge voltage (Vd/2) as a reference voltage. If the signal voltage (V_S) is greater (or smaller) than Vd/2, the output voltage that is amplified with the sense amplifier will be Vd (or 0), respectively. The read operation is completed when the amplified voltage corresponding to the information is turned on by the column selector signal (Y0) so that it is provided as an output to the outside. In this case, the information about all the non-select memory cells (M1) on the select word line is read and sent to each data line, where the information will be amplified by each sense amplifier. At the end of this read operation, therefore, the information in the memory cells will have been destroyed. As a result, the signal voltage that has been amplified by the sense amplifier must be rewritten into each memory cell (Figure 2-3).

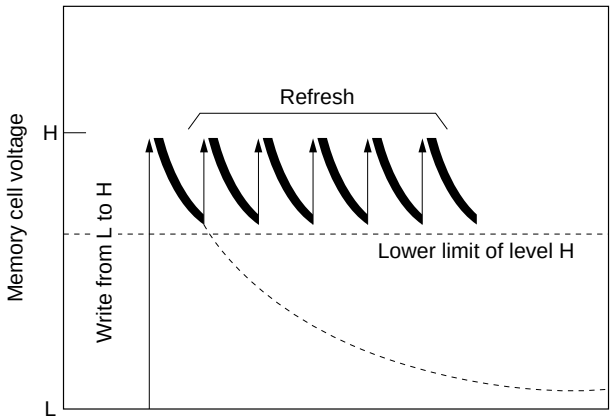


Figure 2-3 Refreshing DRAM Memory Cells

(3) Write Operation

To prevent the information in the non-select cells from being destroyed, the write operation into the select memory cells (M0) proceeds as follows. Writing is first preceded by reading with respect to all memory cells on WL0. Each data line once holds the cell amplifier voltage. The column selector switch is turned on, the amplifier voltage on the selected data line D0 is forcibly replaced with the write information voltage from the outside (I/O), and the voltage is applied to the selected cell's capacitor. Meanwhile, the amplifier voltages at the other non-select data lines are re-written into all non-select cells at the same time. During either a read or write operation, therefore, the non-select memory cells on the same word line undergo a series of reading minute signals, amplifying them, and rewriting them.

2.3 Refreshing DRAM

DRAM memory cells make full use of the high impedance of MOS devices so that the degree of integration may be increased with fewer elements. This requires refreshing. Since the principle of refreshing was mentioned earlier, this section details the different modes of refreshing.

Application

DRAM refreshing is performed by gaining access to all word lines within a predetermined interval, called the "refresh period." The refresh period and the number of word lines, which corresponds to the number of refresh cycles, are different depending on product types. See Table 2-1, which lists the individual DRAM products refreshed at Hitachi.

Table 2-1 How Individual DRAM Products Are Refreshed at Hitachi

Type	Memory structure	Refresh cycle	Refresh period	Refresh address	$\overline{\text{RAS}}$ only refresh	CBR refresh	Self refresh
HM5116100	16M × 1	4k	64ms/128ms	A0 to A11	O	O	O
HM5116400	4M × 4	4k	64ms/128ms	A0 to A11	O	O	O
HM5117400	4M × 4	2k	32ms/128ms	A0 to A10	O	O	O
HM5117800	2M × 8	2k	32ms/128ms	A0 to A10	O	O	O
HM5116160	1M × 16	4k	64ms/128ms	A0 to A11	O	O	O
HM5118160	1M × 16	1k	16ms/128ms	A0 to A9	O	O	O
HM5165400	16M × 4	4k	64ms/128ms	A0 to A11	O	O	O
HM5164400	16M × 4	8k	64ms/128ms	A0 to A12	O	O	O
HM5165800	8M × 8	4k	64ms/128ms	A0 to A11	O	O	O
HM5164800	8M × 8	8k	64ms/128ms	A0 to A12	O	O	O
HM5165160	4M × 16	4k	64ms/128ms	A0 to A11	O	O	O
HM5164160	4M × 16	8k	64ms/128ms	A0 to A12	O	O	O

(1) Refreshing Method

(a) Centralized and decentralized modes

For example, 16-megabit DRAM requires a 4k refresh cycle within 64 ms. If the 4k refresh cycle is carried out continuously, the processing is called the "burst refresh" or centralized mode. If one cycle is carried out at an interval of 15.6 us (that is, 64 ms divided by 4k), the processing is called the "distributed refresh" or decentralized mode.

(b) Synchronous and asynchronous modes

The asynchronous mode refers to the method of assigning the usual time for reading or writing to refreshing, as necessary. If the time for refreshing is assured in advance, the method is called the synchronous mode. The asynchronous mode is suitable for high-speed systems, because it is possible to insert refresh cycles effectively. If the processor's bus cycle is relatively long, the synchronous mode allows system design to be carried out without considering the refresh-related wait time. These characteristics may be summarized as in Table 2-2. You should select the most efficient mode according to the characteristics of your system.

Table 2-2 Refresh Methods Compared

	Centralized mode		Decentralized mode	
Refresh method	**Synchronous**	**Asynchronous**	**Synchronous**	**Asynchronous**
Memory system dead time	No	Yes	No	Yes
Maximum wait time	No	4,096 or 8,192 cycle	No	One cycle
Memory system cycle time	Slow	Fast	Slow	Fast

(2) Refresh Mode

See Table 2-3, which compares the various refresh modes for DRAM. We also give the detailed description of each mode.

(a) $\overline{\text{RAS}}$ only refresh

In refreshing, there is no need to enter column addresses, because it requires only selection of word lines (conducted by row addresses). The term "$\overline{\text{RAS}}$ only refresh" refers to refreshing by entering only row addresses in synchronization with $\overline{\text{RAS}}$. As compared with ordinary access, $\overline{\text{RAS}}$ only refresh requires low power consumption and allows the output terminal to keep providing high impedance.

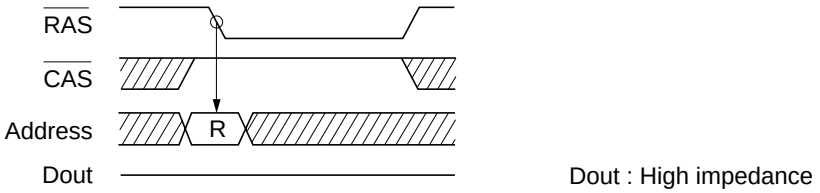
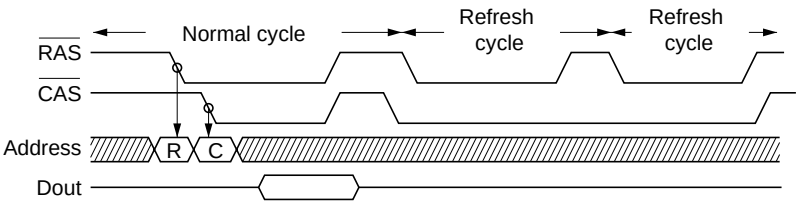
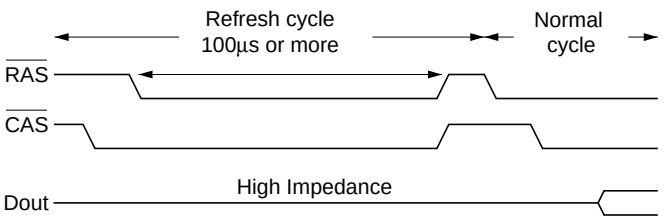
(b) $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh

This mode does refreshing by starting $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$. Since chips have a built-in refresh address counter, there is no need to enter refresh addresses from the outside. In system design, it is possible to simplify the external address multiplexer. The output terminal keeps high impedance.

(c) Self-refresh mode

$\overline{\text{CAS}}$ is started before $\overline{\text{RAS}}$, and $\overline{\text{CAS}}$ is held at its low state for at least 100 ms before the refresh mode starts. Once this mode starts, the chip's refresh address counter and fresh timer both start operating. The chip itself carries out refreshing at a regular interval. In system design, the built-in timer and counter help significantly simplify the external control section. If, with the system standby, you use the self-refresh mode, the memory itself performs refreshing automatically. It is thus possible to separate the power-consuming processor, leading to power saving. The chip itself, of course, performs low self-refresh currents through the extremely long internal refresh cycle.

Table 2-3 Comparing DRAM Refresh Modes

$\overline{RAS}$ only refresh	
$\overline{CAS}$-before-$\overline{RAS}$ refresh	
Self refresh	

(3) Setting Refresh Addresses

Through a combination of the same refresh address, you can easily upgrade your memory for devices with different capacities or bit configurations. If you refer to Table 2-1 for a comparison of refresh addresses, you can replace those 4M × 4, 4k refresh cycle products with those 4M × 16, 4k refresh cycle products — without having to change the processor control method.

2.4 High-Speed Access to DRAM

DRAM usually has a disadvantage that it is slower than SRAM in terms of access time and cycle time. Therefore, we support various modes of high-speed access to increase access time efficiently. DRAM reading proceeds in the following sequence. First, the row address selects a word line. All the data in the memory cells connected to the word line is sent to the sense amplifier. Next, the column address selects some of the sense amplifiers, and the data in them is sent to the output buffer. Once the output of the sense amplifier has been determined, therefore, all you have to do is to change column addresses if you want to access the data in another memory cell. High-speed access provides access through changes in column address; the data is only sent from the sense amplifier to the output terminal. This means shorter access time than in ordinary cycles.

See Figure 2-4, which compares various modes.

(1) Page Mode

With the $\overline{RAS}$ signal at L, the $\overline{CAS}$ signal is entered as a clock. In synchronization with the $\overline{CAS}$ signal, it is possible to read the data in the memory cells connected to the word line selected by the row address.

(2) Fast Page Mode

This is today's standard mode for DRAM. The function of the above page mode applies, of course. And with the $\overline{CAS}$ signal at H, the address is secured. This reduces the $\overline{CAS}$ signal's access time from the falling edge, as well as the $\overline{CAS}$ cycle time.

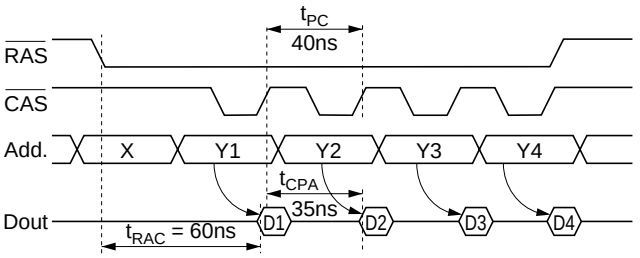
(3) Extended Data Output (EDO) Page Mode

This mode gives the fast page mode an improvement in data transfer rate. Previously, DRAM used an output control method in which the $\overline{CAS}$ signal is started to put the output data during the read cycle into high impedance. By contrast, the current method is such that the output data can be held even if the $\overline{CAS}$ signal is set at the H level. As a result, it is possible to reduce the cycle time as compared with the fast page mode.

Synchronous DRAM will be one of the high-speed DRAM products available in the near future.

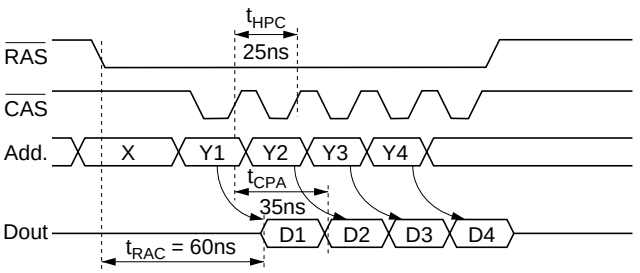
Different from the existing DRAM products, synchronous DRAM is given a new capability that enables high-speed data transfer. Its operation is controlled with commands. Both the command input and data input/output operations are synchronized with the start of external clock signals. The burst mode enables continuous data input/output operations in synchronization with clock signals. Synchronous DRAM is detailed in Chapter 3.

Fast page mode



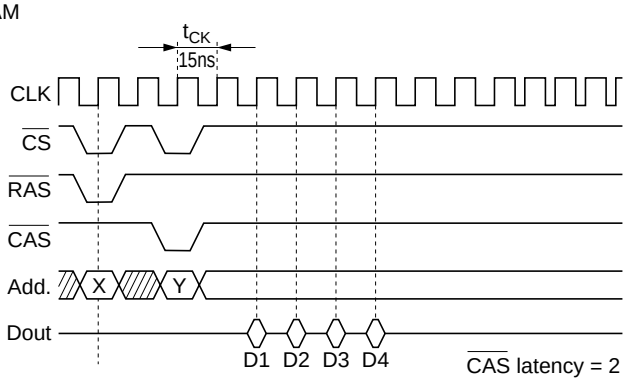
(Corresponding system clock 25MHz)

EDO page mode



(Corresponding system clock 40MHz)

SDRAM



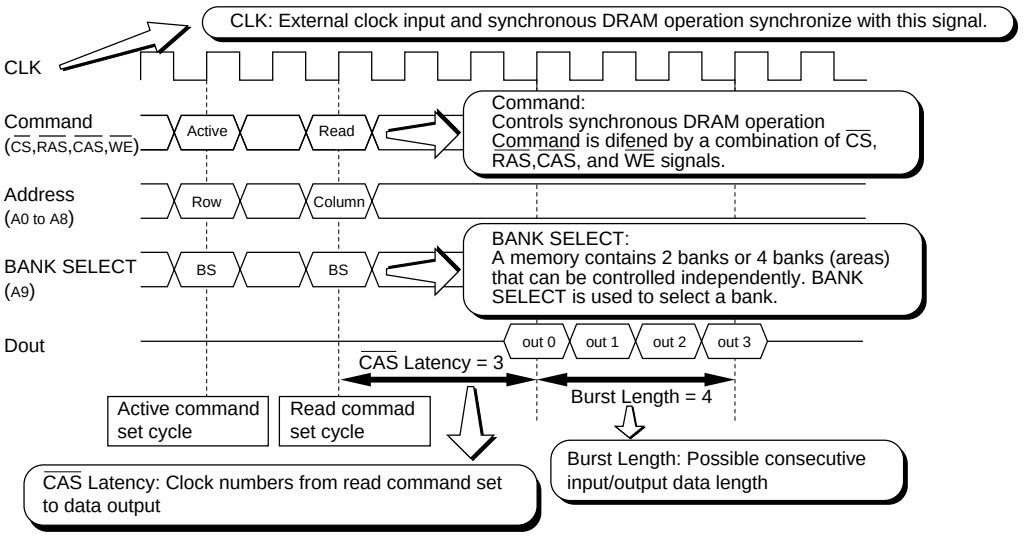
(Corresponding system clock 66MHz)

t_{CPA} : Access time measured from $\overline{CAS}$ precharge operation
t_{PC} : Cycle time in fast page mode
t_{HPC} : Cycle time in EDO page mode
t_{CK} : System clock cycle time

Figure 2-4 Comparing High-Speed Access Mode Timings

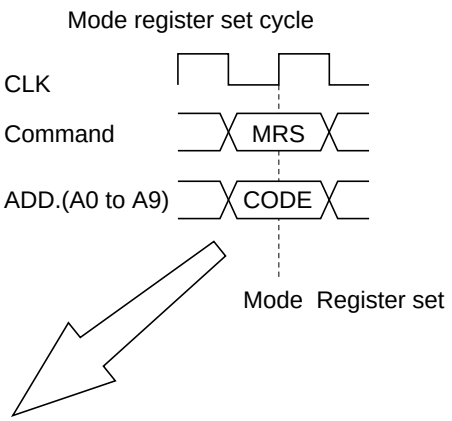
3. Operation and Usage of SDRAM

3.1 Keywords



3.2 Mode Register Set

Mode Register is set using the mode register set (MRS) command and address pins.



Specification of address pins

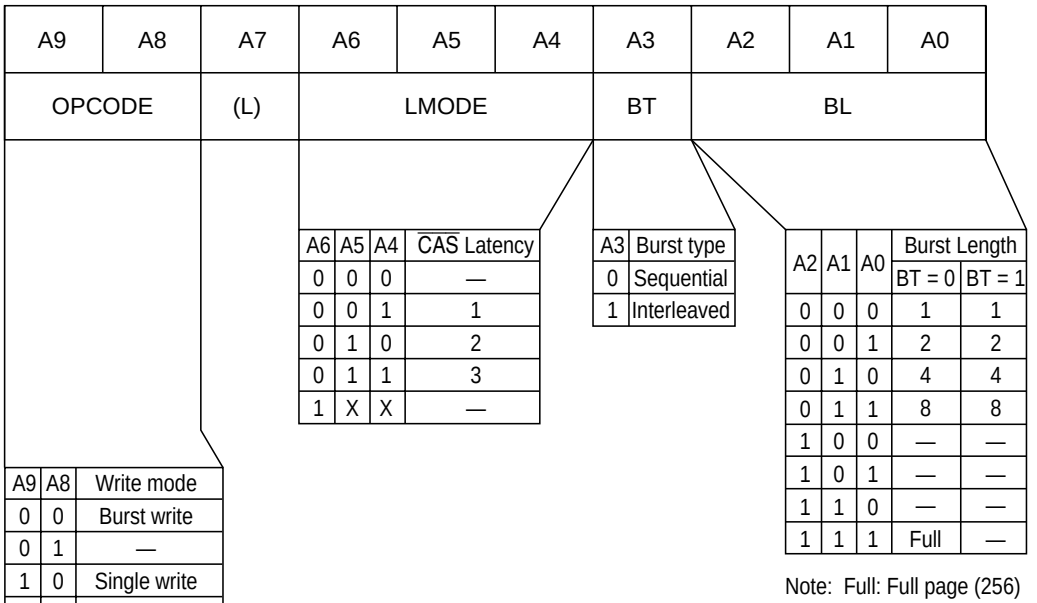
A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
OPCODE		–*1	LMODE			BT	BL		

Note: 1. Pin A7 is always used with "L" in mode register set.

3.3 Mode Register

Mode Register: Sets information on SDRAM operation mode

Setting items of mode register



A9	A8	Write mode
0	0	Burst write
0	1	—
1	0	Single write
1	1	—

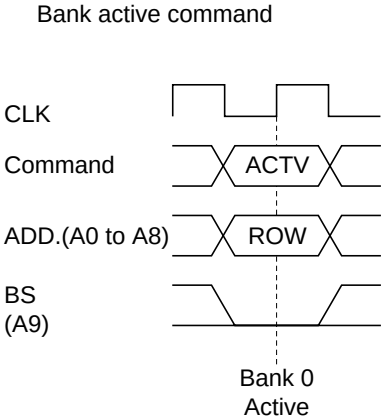
A6	A5	A4	$\overline{CAS}$ Latency
0	0	0	—
0	0	1	1
0	1	0	2
0	1	1	3
1	X	X	—

A3	Burst type
0	Sequential
1	Interleaved

A2	A1	A0	Burst Length	
			BT = 0	BT = 1
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	—	—
1	0	1	—	—
1	1	0	—	—
1	1	1	Full	—

Note: Full: Full page (256)

3.4 Bank Active



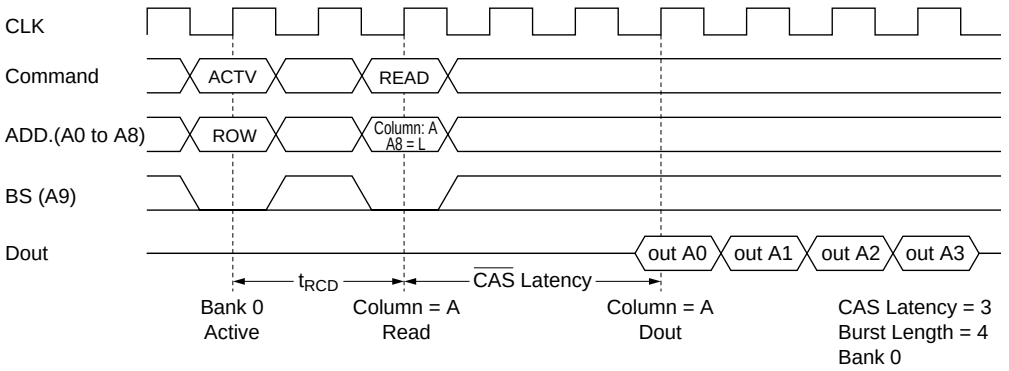
The bank specified by BS (A9) is selected,and activates the ROW address (word line) specified by address (A0 to A8).

Wait state of read or write command input

BS (A9) = "L" → Selects bank 0
BS (A9) = "H" → Selects bank 1

3.5 Read

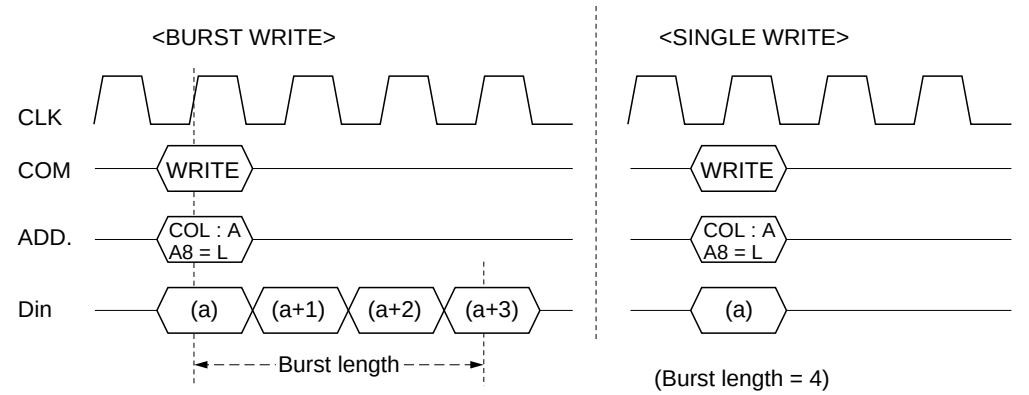
Read cycle



- t_{RCD} or more is required during Active-Read command.
- Data is output after the $\overline{CAS}$ Latency cycle, which follows the Read command input.
- Data, whose length is set by Burst Length, is output in synchronization with the clock.
- After output of the last data, the output buffer automatically goes to high impedance.

3.6 Write

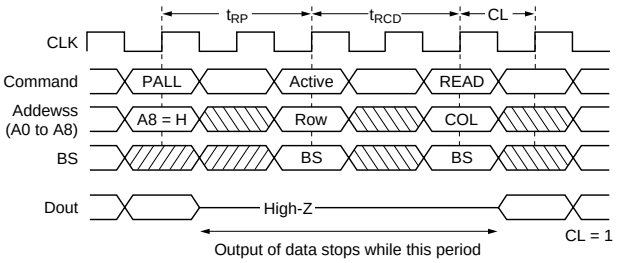
The write operation mode is set to burst write or single write by the mode register.



- Data of Burst Length is written in the burst write mode.
- Data is written in 1 address space only, regardless of the Burst Length, in the single write mode.

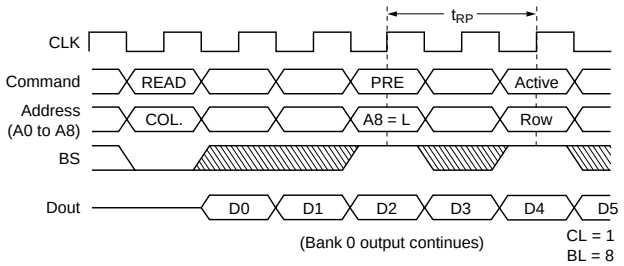
3.7 Precharge

1. Precharge All Banks



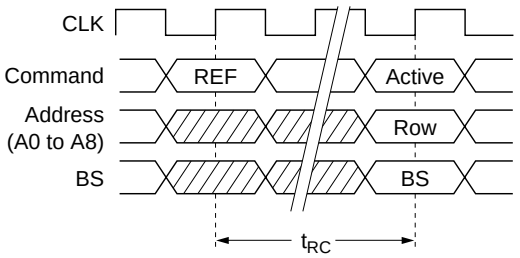
- Setting A8 = H starts the precharge operation of both banks (bank 0, 1) regardless of BS (A9).
- Next Active command for any bank is set after t_{RP}.

2. Precharge Selected Bank



- The bank specified by BS (A9) starts precharge operation.
- Active command for the same bank is set after t_{RP}.
- Commands for other banks start at next cycle.

3.8 Auto-refresh



- After refresh operation has started, specification of refresh address is not required. (Address is internally generated.)
- Next Active command is set after t_{RC}.
- Refresh cycle : 1 k/16 ms
  (Refresh of all ROW addresses takes 1024 cycles.)

4. Synchronous Graphic RAM

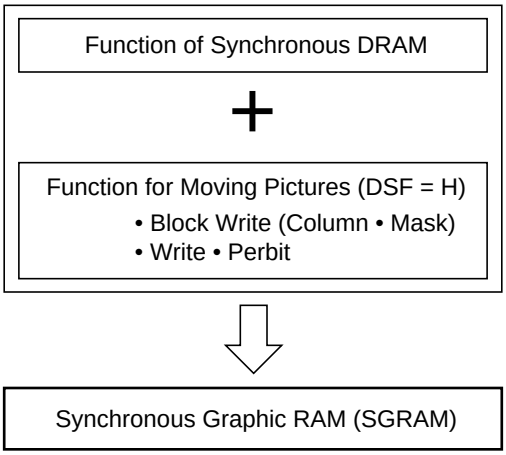


Figure 4-1 A General Concept of Synchronous Graphic RAM

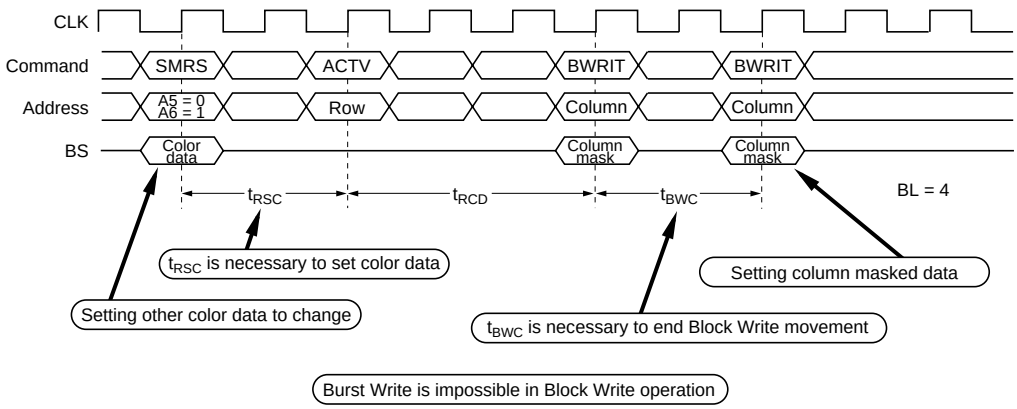


Figure 4-2 Block Write Operation

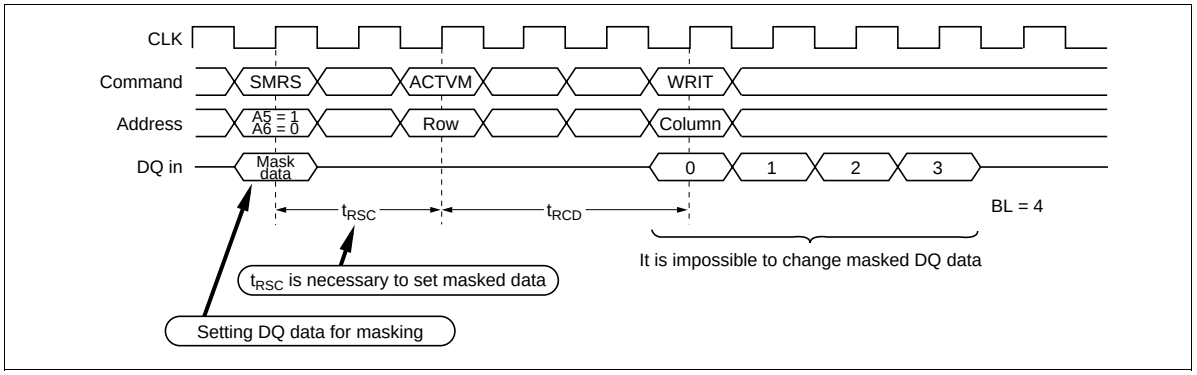


Figure 4-3 Write Perbit Operation

5. Instructions for Using Memory Devices

5.1 Prevention of Electrostatic Discharge

As semiconductor memory designs are based on a very fine pattern, they can be subject to malfunction or defects caused by static electricity. Though the built-in protection circuits assure unaffected reliability in normal use, devices should be handled with these precautions:

1. In transporting and storing memory devices, place them in a conductive magazine or wrapper, or put all pins of each device into a conductive mat, so that they are kept at the same potential. Manufacturers should give sufficient consideration on proper packing when shipping their products.
2. When the devices are to be touched during mounting or inspection, the handler must be grounded. Do not forget to connect a resistor (1 MΩ approximately is desirable) in series for protect 10 n against electrical shock.
3. Keep the relative ambient humidity at about 50% during processing.
4. For working clothes, cotton is preferable to synthetic fabrics.
5. Use a soldering iron operating at low voltage (12 V or 24 V, if possible) with its tip grounded.
6. When transporting a board with memory devices mounted on it, enclose it with conductive materials.
7. Use conductive materials of high resistance (about 109 ohms) to protect the devices from electrostatic discharge. Otherwise, if accident-ally put in contact with conductive materials such as a metal sheet, the devices may deteriorate or even breakdown, owing to the sudden release of charge stored on the surface.
8. Never set a system in which memory devices are used near anything that generates high voltage (e.g., a CRT anode electrode, etc.).

5.2 Using CMOS Memories

As shown in Figure 5-1, the input of a CMOS memory is connected to the gate of an inverter consisting of PMOS and NMOS transistors. Figure 5-2 shows the relationship between the input voltage and current within the inverter. The top and bottom transistors turn on and create a current flow when the input voltage reaches an intermediate level. Therefore it is necessary to keep the input voltage below 0.2 V or above V_{CC} - 0.2 V in order to minimize power consumption. The data sheet specifies the standby current for two cases of input level (with minimum V_{IH} and maximum V_{IL}, and with 0.2 V or V_{CC} - 0.2 V), and the difference in values as being remarkably great. Some memory devices are designed to cut off such current flow in the standby mode by the control of input signals, but this depends on the specific device type. This should be confirmed in data sheets for each device type.

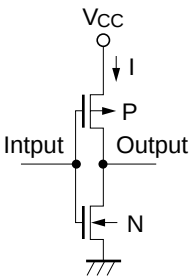


Figure 5-1 CMOS Inverter

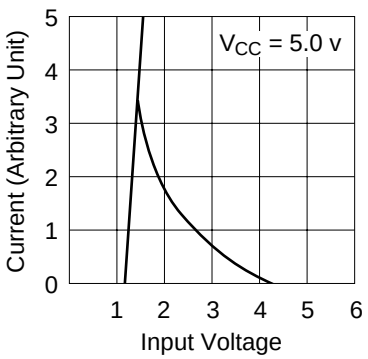


Figure 5-2 Relationship Between Input Voltage and Current in a CMOS Inverter

Another problem peculiar to CMOS devices is latch up. Figure 5-3 shows the cross section of a CMOS inverter and the structure of a parasitic bipolar transistor. The equivalent circuit of the parasitic thyristor is shown in Figure 5-4. When positive DC current or pulse noise is applied (Figure 5-4a), T_{R3} is turned on owing to the bias voltage generated between the base and emitter. Also, trigger current flows to ground through R_P, the base resistance of T_{R2}. As a result, T_{R2} becomes conductive and the current flows from power supply (V_{CC}) through the base resistance of T_{R1} (R_N), which also puts T_{R1} into conduction. Then as the base of T_{R2} is rebiased by the collector current from T_{R1}, the closed loop consisting of T_{R1} and T_{R2} reacts. Thus, current flows constantly between the power supply (V_{CC}) and ground even without the trigger current caused by outside noise.

Application

Latch up can also be caused by a negative pulse (Figure 5-4b). Most semiconductor memory manufacturers are trying to improve latch up immunity in their products. Hitachi provides a broad enough guard band by applying a diffusion layer around the inputs and outputs, taking care not to connect the input to the p^+ diffusion layer. The input voltage for the 64-kbit static RAM HM62256, for example, is specified as follows:

V_{IH} max 6.0 V (not dependent on V_{CC})
V_{IL} min 3.0 V (pulse width = 50 ns)
-0.5 V (DC level)

Thus almost no consideration for latch up is required in system designs using these devices.

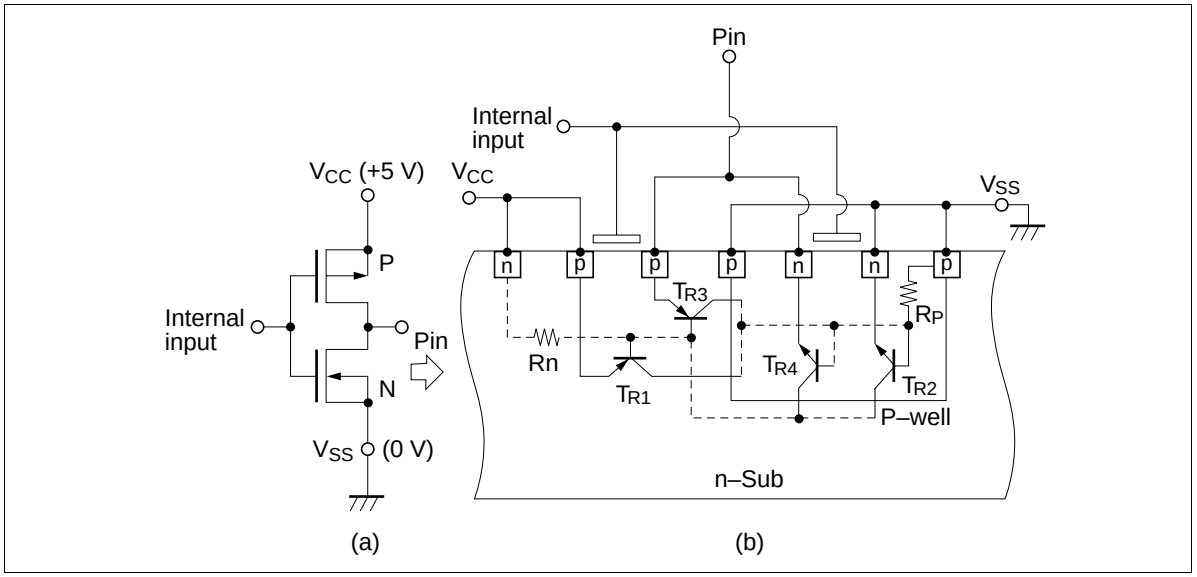


Figure 5-3 Cross Section Structure of CMOS Inverter

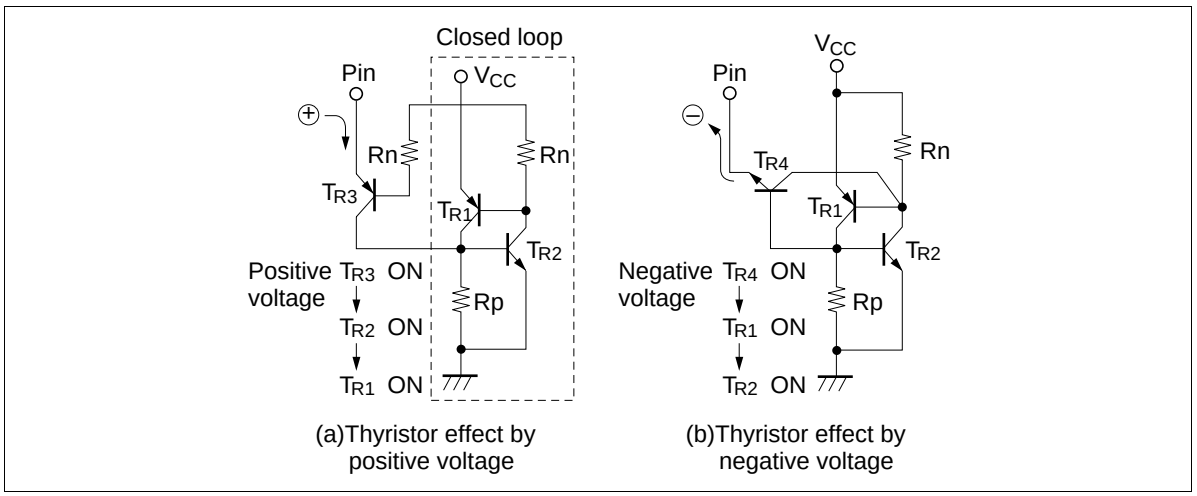


Figure 5-4 Equivalent Circuit of Parasitic Thyristor

5.3 Noise Prevention

Noise in semiconductor memories is roughly classified as input signal noise and power supply noise.

Input Signal Noise: Input signal noise is caused by overshoot and undershoot. If either of them exceeds the recommended DC operating conditions, normal operation is hindered, and a voltage over the absolute maximum rating will break the device. When operating high speed systems, special care is required to prevent input signal noise.

The noise can be prevented by inserting a serial resistance of less than 50 ohms into each input or a terminating resistance into the input line. Actually, however, input signal noise can be simply reduced by a stable power supply line, because the noise is often caused by an unstable reference voltage (ground level).

Power Supply Noise: Power supply noise can be classed as low-frequency and high-frequency as shown in Figure 5-5. To assure a stable memory operation, combined low- and high-frequency noise should be held below 10 percent of the standard level of the peak-to-peak power supply voltage.

Devices like dynamic RAMs, which operate from clock signals, or high speed CMOS static RAMs, through which current flows during the transition of signals, consume high peak current. When a power supply does not have enough capacity for the peak current, the voltage drops. And if the recovery rate of the power supply synchronizes with its time constant, it may start oscillating. To reduce the influence of the peak current, a bypass capacitor of 0.1-0.01 μF should be inserted near the device. The following points must be considered in designing the layout of a board:

1. For bypass capacitors, use titanium, ceramic, or tantalum capacitors which have better high-frequency characteristics.
2. Bypass capacitors must be applied to the power supply pins of memory devices as near as possible, and inductance in the path from the V_{CC} pin to V_{SS} pin through the bypass capacitor must be kept as low as possible.
3. The line connected to the power supply on the board should be as wide as possible.
4. It is preferable for the power supply line to be at right angles to devices selected at the same time, otherwise too much peak current will flow through one power supply line at a time.

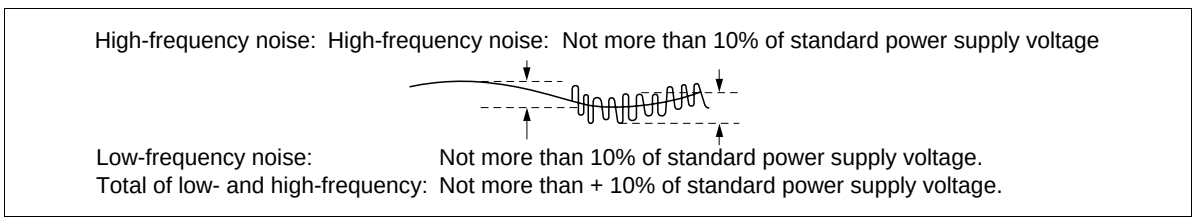


Figure 5-5 Power Supply Noise

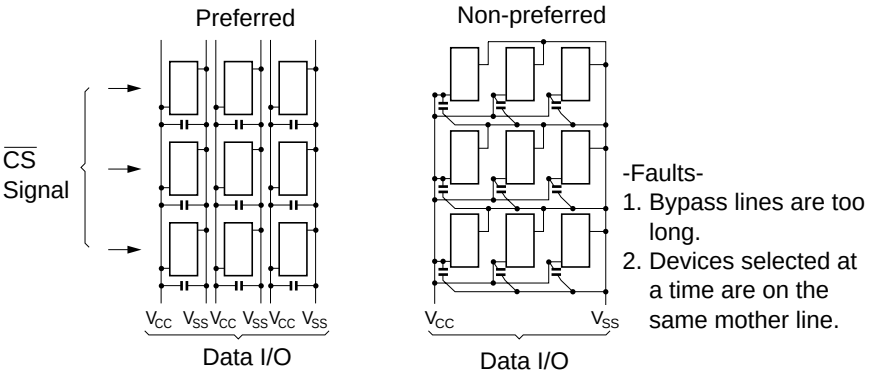


Figure 5-6 Examples of a Power Supply Board Pattern

6. Referential application note

- Synchronous DRAM

1. Flash Memory

1.1 Features and Application of Flash Memory

Among a variety of large-capacity memory technologies, flash memory provides three major features, as illustrated in Figure 1-1. They are (1) lower power consumption and high reliability in tough environments, in terms of vibration, shock, and temperature range; (2) a function to rewrite in system installation; and (3) being nonvolatile. Because of these features, flash memory is expected to replace the existing products (such as DRAM, ROM, HDDs, and FDDs) mainly in the growing market for portable information devices (see Figure 1-2).

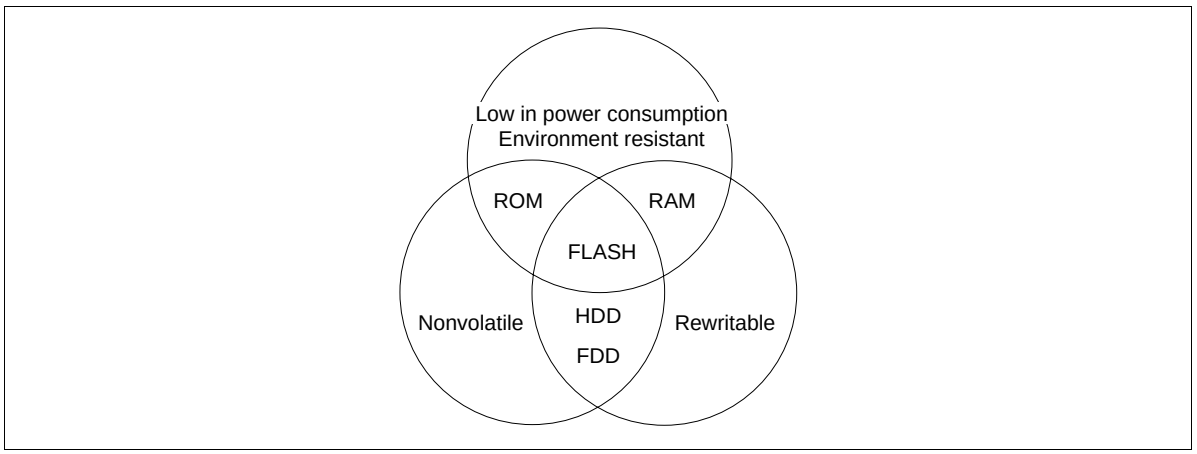


Figure 1-1 Major Features of Flash Memory

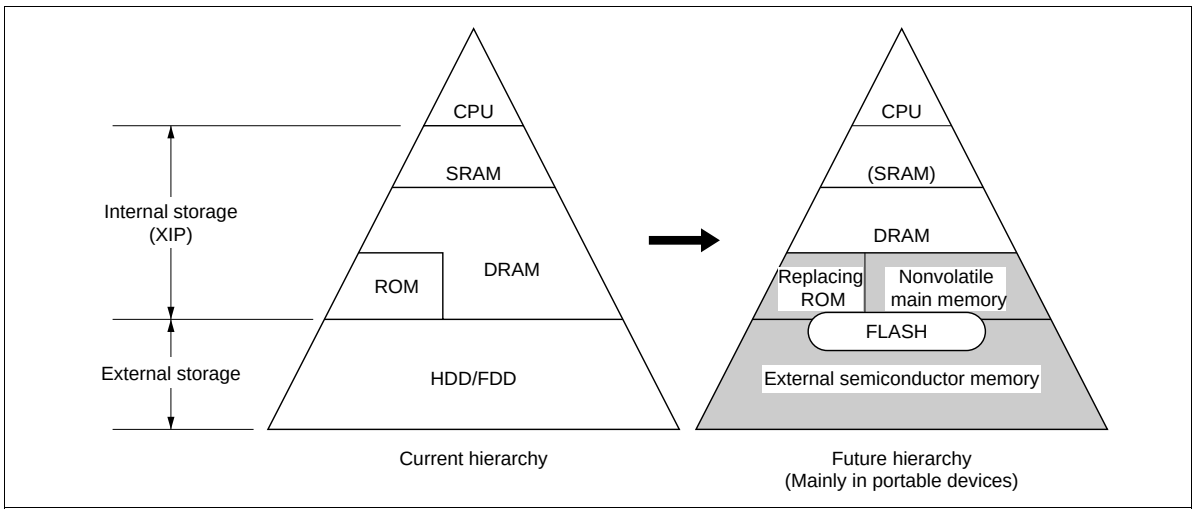


Figure 1-2 Computer's Memory Hierarchy

Application

The application of flash memory falls under two major categories. In the first category, flash memory, as with DRAM or RAM, is connected to a system bus, so that the CPU gains direct access to the flash memory used as internal storage. The second category refers to external storage that is equivalent to an HDD or FDD connected to an external bus through an interface. These modes of application are expected to play a major role in the growing flash memory market.

It should be remembered that different modes of application call for different requirements. When used as internal storage, flash memory must provide high-speed random reading, which enables direct run called "execute in place" (XIP). When used as external storage, meanwhile, flash memory should meet the capability of rewriting data on a 512 bytes basis, which is equivalent to the capability of an HDD or FDD. See Figures 1-3 and 1-4.

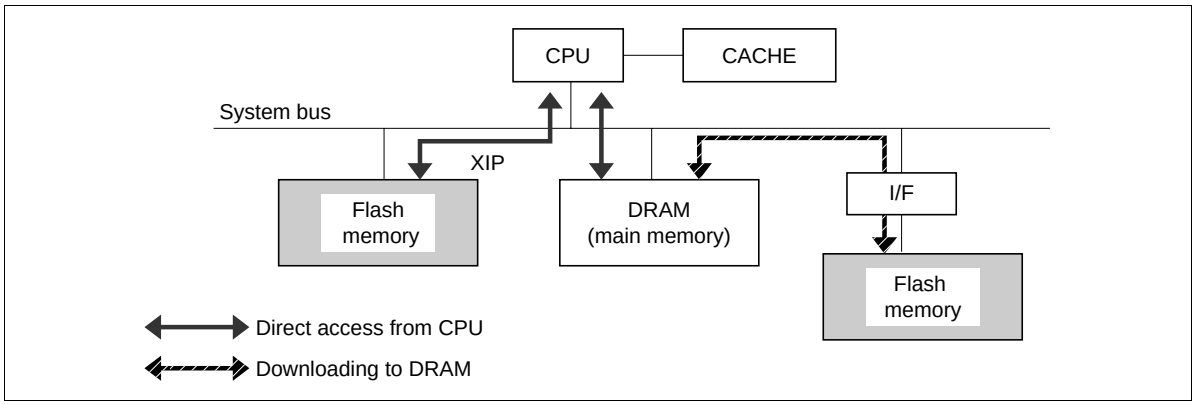


Figure 1-3 Application of Flash Memory

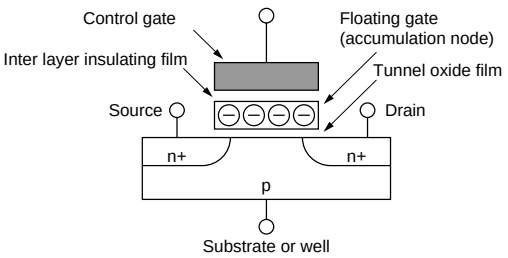
Field of application		Contents of storage	Required performance
Internal storage (XIP)	Rewriting ROM	Boot code, BIOS, fonts	High speed random reading; Single low voltage power supply
	Rewriting DRAM	Operating System, application programs, data	
External storage	Rewriting HDD	Operating System, application programs, data	High degree of integration; Small block size

Figure 1-4 Requirements for Flash Memory

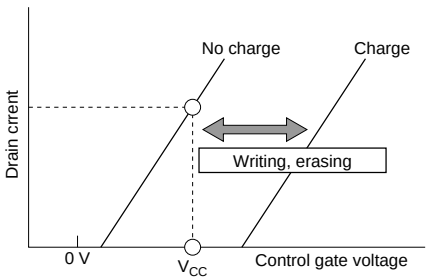
1.2 Features of AND-Type Flash Memory

Flash memory has been available in different types of elements, including AND, NOR, NAND, DINOR, and HICR. These types may be classified, as in Figures 1-5 and 1-6, from the following three aspects:

(1) Connection: How to arrange cells between data and source lines
(2) Logic: Relationship between the memory element's high/low value of voltage (Vth) and the write/erase operation
(3) Operation: Injecting/removing electrons into/from the floating gate



(a) Basic structure



(b) Change in V_{th} due to floating gate charges

Concept of classification

Connection : How to arrange cells between data and source lines

Logic : Relationship between the high/low value of voltage (V_{th}) and the write/erase operation

Operation : How charges move between the floating gate and substrate

Figure 1-5 How Flash Memory Elements Work

Method	Classification
Connection	Direct connection ---------- NAND Parallel connection ---------- NOR Hierarchical data lines ---------- DINOR Hierarchical data/source lines ---------- HICR AND
Logic	High Vth value in rewriting ---------- NAND NOR Low Vth value in rewriting ---------- DINOR HICR AND
Writing/ erasing	Hot electron injection, tunnel release ---------- NOR Tunnel injection, tunnel release ---------- NAND DINOR HICR AND

Figure 1-6 Classification of Flash Memory Cells

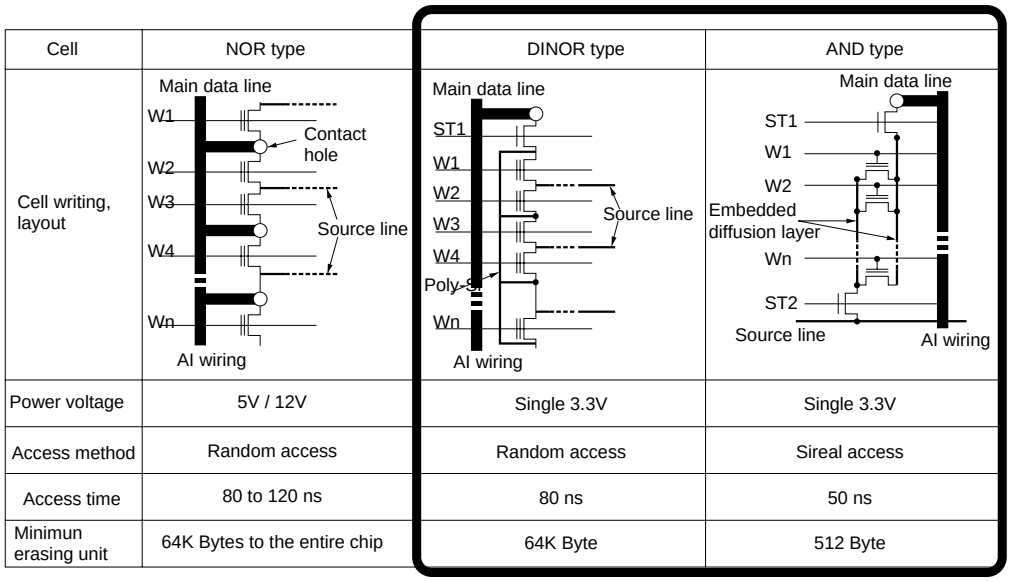
Application

The AND type provides a parallel method for hierarchical data and source lines, while the DINOR type provides a parallel method for hierarchical data lines. Both types feature a logic method that provides a low Vth value during writing and an operation method that provides writing or erasing with FN tunnels (see Figure 1-7). Because of these technical features, the AND type of flash memory enables high-speed reading (serial access). Under a single low-voltage power supply (3.3V), it also implements a higher degree of integration and a small unit of rewriting (the same unit for writing and erasing), which is considered important when used as external storage. For these reasons, Hitachi employs AND-type cells for large-capacity flash memory. Incidentally, the term "AND-type" comes from the fact that the method of connection is parallel connection as with the NOR type, but the method of logic is opposite to the NOR type. The DINOR type enables high-speed reading (random access). It has implemented a single low-voltage power supply (3.3V) for the XIP application involving the CPU's direct access. Hitachi employs DINOR-type cells for small- or medium-capacity flash memory.

Method	Technical feature	Effect	Performance
Connection	Hierarchical data and source lines	Disturbing suppressed	Small block size (writing = erasing)
	Parallel connection	Large reading cell current	High speed reading (serial access)
Logic	Low Vth value in rewriting		
Operation	Using FN tunnels	Lower current operation	Single low voltage power supply (3.3V)
Process	Diffusion layer wiring	Contactless structure	High degree of integration

Figure 1-7 Features of AND-Type Flash Memory

See Figure 1-8, which illustrates AND-type and DINOR-type memory cells.



Cell	NOR type	DINOR type	AND type
Cell writing, layout			
Power voltage	5V / 12V	Single 3.3V	Single 3.3V
Access method	Random access	Random access	Sireal access
Access time	80 to 120 ns	80 ns	50 ns
Minimun erasing unit	64K Bytes to the entire chip	64K Byte	512 Byte

Figure 1-8 Features of Individual Cell Methods

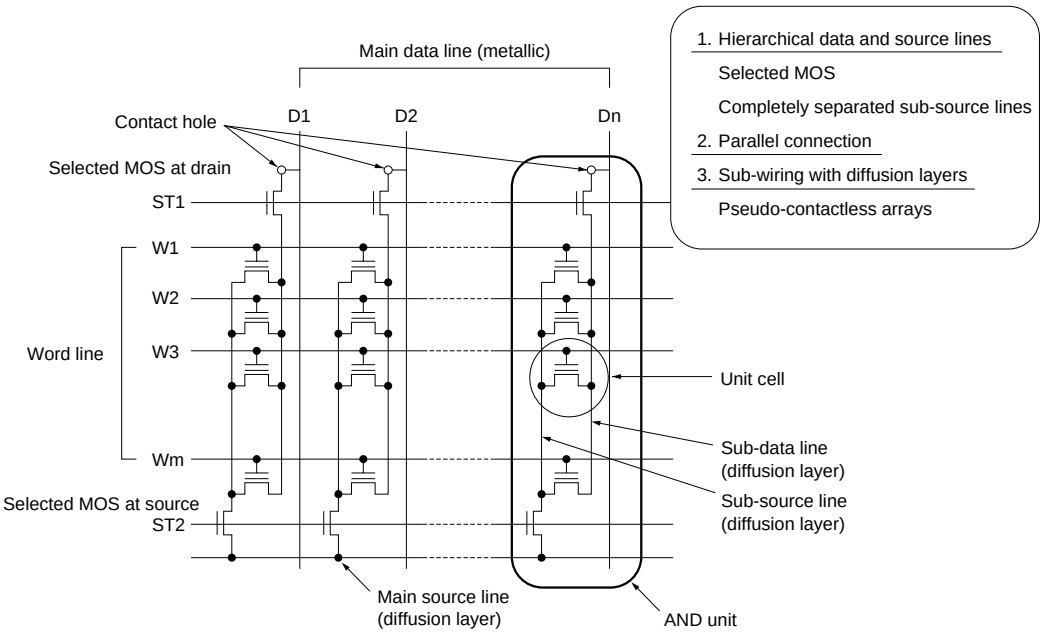


Figure 1-9 AND-Type Memory Array Circuit

Application

The AND unit consists of "m" unit cells, which are connected in parallel between the sub-data line and the sub-source line, and two selected transistors, which are used to connect the sub-wiring to the main wiring. The memory array can be characterized by the following: (1) parallel connection of memory cells; (2) wiring with hierarchical data and source lines; and (3) a pseudo-contactless structure using diffusion layers to form the sub-wiring. By connecting memory cells in parallel, it is possible to produce a memory current (at least 20 uA) required for high-speed random reading, as with the NOR type. Regarding the wiring hierarchy, the selected transistor on the drain side separates the AND unit from the main data line. This helps remarkably reduce the capacity of the main data line, making it useful for higher speeds and lower power consumption. Meanwhile, the selected transistor on the source side separates the sub-source line from the main source line. This helps reduce the capacity and gives a complete 1:1 relationship with the data line. As a result, it is possible to implement a small block size (roughly 512 bytes), in which the unit of writing is exactly the same as the unit of erasing, without any influence from the disturbance.

In the following, we discuss the effort to reduce voltage.

(1) The AND and DINOR types can operate from a single external low-voltage power supply because writing or erasing requires only a small operating current. As compared with the value of a current (ranging from 100 uA to 1 mA) that is practically available from the on-chip built-in power supply, the operating current for AND-type cells is fairly small — not larger than 50 nA per bit. This can implement a write or erase operation from a single 3.3V power supply even if you consider a parallel operation handling roughly 512 bytes.

(2) In terms of reading, the AND and DINOR types are suitable for producing a lower-voltage power supply (not higher than 3.3V). Because the lower threshold voltage for memory cells is implemented in writing, when the read voltage is lowered from the previous 5V to 3.3V, it is possible to control the end points of individual memory cells, depending on the characteristics. This helps reduce the control range for the lower threshold voltage. As a result, it is possible to, at the same time, secure the memory cell read current and prevent the deplete trouble from taking place, thus enabling high-speed reading at low voltage.

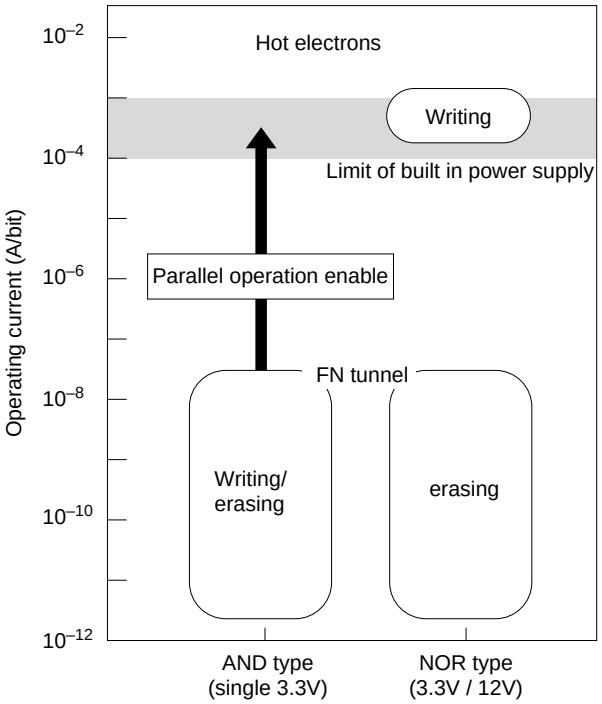


Figure 1-10 Operating Current in AND-Type Flash Memory Cells

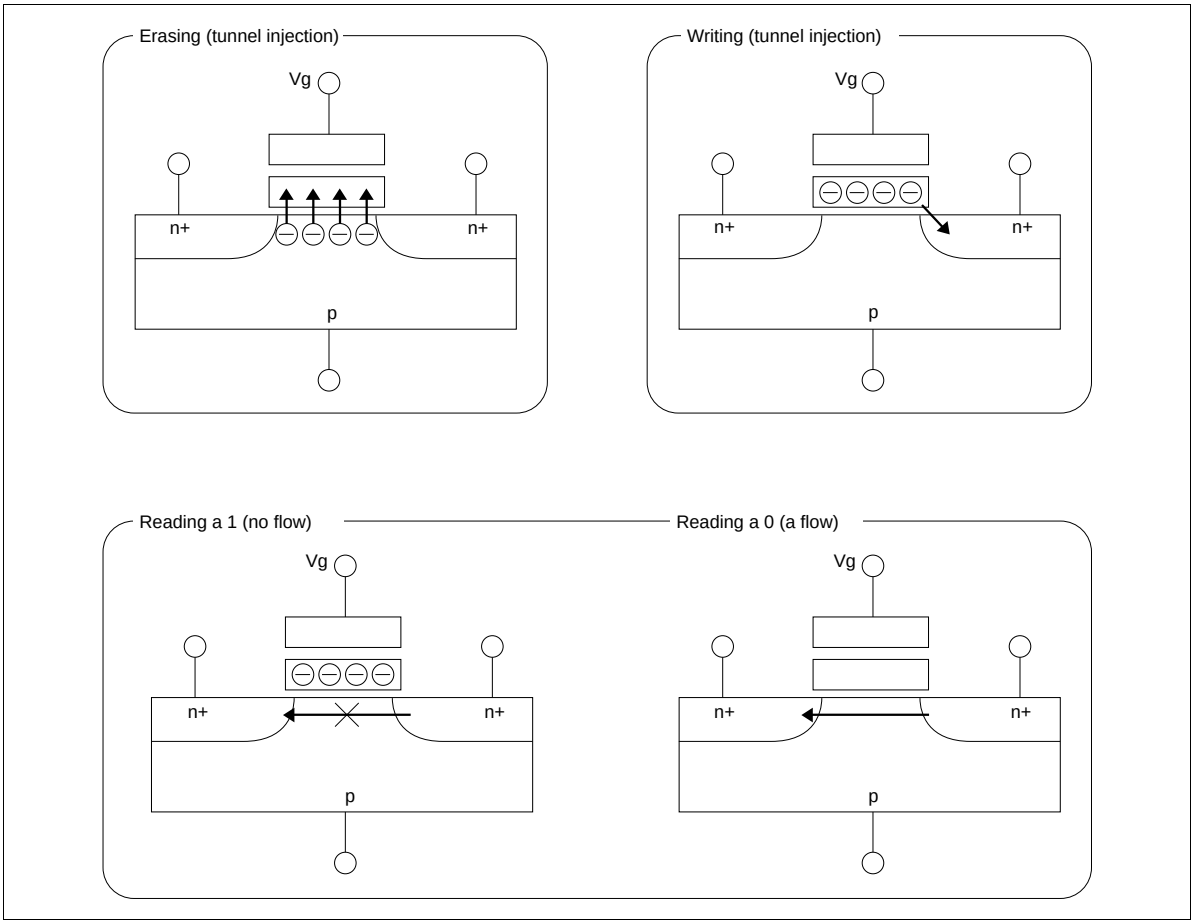


Figure 1-11 Basic Operation of AND-Type Flash Memory Cells

2. EEPROM

2.1 EEPROM Memory Cell

An EEPROM is an electrically erasable and programmable ROM which can be erased or written remotely while the system is in operation.

Hitachi EEPROM memory cells are MNOS-type (Metal Nitride Oxide Semiconductor) as shown in Figure 2-1.

A MNOS memory cell consists of two layers of oxide film and nitride film. The thickness of the oxide film is about 20 Å and the nitride film is 200 to 300 Å. There are traps in the boundary of the oxide and nitride films to catch electrons. The electrons move by the tunneling phenomenon between the substrate and traps.

2.2 CMOS EEPROM Function

Page Programming Function: The CMOS EEPROMs can latch page data and write them in single write cycle. The write cycle time is specified as 10 ms (max.). The effective byte programming speed in page write mode is 10 ms/128 bytes = 0.78 μs/byte in case of HN58C1001.

Thus it takes only 10.24 seconds to write the entire HN58C1001. Figure 2-2 shows the internal operation in case of HN58C1001. The following describes the operation sequence:

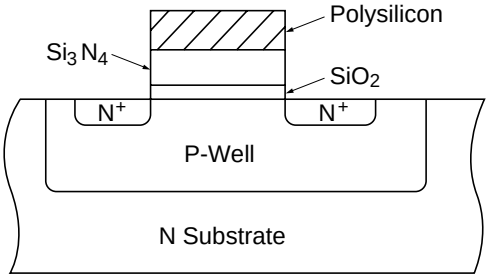


Figure 2-1 MNOS-Type Memory Transistor

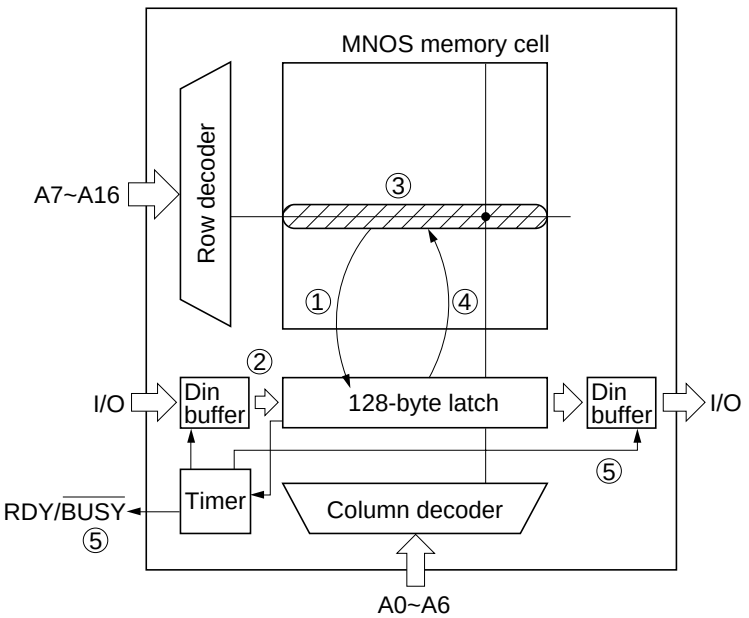


Figure 2-2 HN58C1001 Page Write

1. The 128-byte memory cell data at the row address selected by address pins A7 - A16 are latched.
2. Latched data at the column address specified by address pins A0 - A6 are altered with write data, which is put into the Din buffer from I/O pins I/O0 - I/O7.

   The 128 bytes (max.) of latched data are altered by repeating this operation 128 times.

3. 128 bytes of memory cell data in the selected row 1 are erased (all set to 1).
4. Latched data is written into the selected row 3.
5. CPU acknowledges completion of the write cycle based on the internal timer. The HN58C1001 provides RDY/$\overline{\text{BUSY}}$ and $\overline{\text{DATA}}$ polling to indicate the write completion.

Internal Timer: The CMOS EEPROMs indicates the completion of a data write to the CPU by using an internal timer. They enter the next cycle as soon as the completion of the write is detected. This function offers a high system throughput as the CPU can access other devices during a write cycle. They have two functions, RDY/$\overline{\text{BUSY}}$ and $\overline{\text{DATA}}$ polling, to indicate the completion of data write.

The RDY/$\overline{\text{BUSY}}$ approach indicates the completion of data write by using pin 1. It is low when the HN58C1001 is in data write operation ($\overline{\text{BUSY}}$) and turns to the high impedance state at the end of data write (RDY). The RDY/$\overline{\text{BUSY}}$ pin should be pulled up as it uses open drain output. The RDY/$\overline{\text{BUSY}}$ pins can be OR-wired when using several EEPROMs.

The $\overline{\text{DATA}}$ polling approach, implemented in software, indicates the completion of data write through pin 19 (I/O7). While the data write is not completed, I/O7 shows an inverted version of what was written in the last cycle. In using this approach, the RDY/$\overline{\text{BUSY}}$ pin should be opened or grounded. The $\overline{\text{DATA}}$ polling approach can acknowledge the completion of a data write in an individual EEPROM, even if several HN58C1001's are used in the system.

Data Protection: The EEPROM performs a data write with a higher voltage (V_{PP}) than the power supply voltage (V_{CC}). The CMOS EEPROMs internally generate V_{PP} by a high voltage generator with the combination of control pins ($\overline{\text{CE}}$, $\overline{\text{OE}}$, $\overline{\text{WE}}$). It supports the following functions to avoid accidental data write (data protection).

1. Data protection against noise on the control pins ($\overline{\text{CE}}$, $\overline{\text{OE}}$, $\overline{\text{WE}}$) during operation.
2. Data protection against noise at power on/off.

3. EPROM/OTPROM

3.1 EPROM Programming

Figure 3-1 shows the sectional structure of an EPROM memory cell. The upper gate, one of the gates made of two-layered polycrystalline silicon, is called the control gate and is connected to a word line. The lower layer is called the floating gate and is not connected. This memory cell is programmed as follows.

With the substrate and source grounded, apply a high voltage between the drain and control gate. An electrical potential incline will occur between the source and drain so that the intensity of the electric field will become high near the drain. Because of this electric field, electrons are accelerated and the so-called hot electrons will be generated, which jump over the energy barrier of SiO2 film. The hot electrons are pulled by the electric potential of the control gate and poured into the floating gate. Electrons stored in the floating gate remain stable as they fall into a well surrounded by an energy barrier of SiO_2 film. Therefore, it is evident that the quality of the SiO_2 film surrounding the floating gate is essential for good data retention characteristics. To keep data retention in the 5- or 10-year range, high quality SiO_2 film is needed.

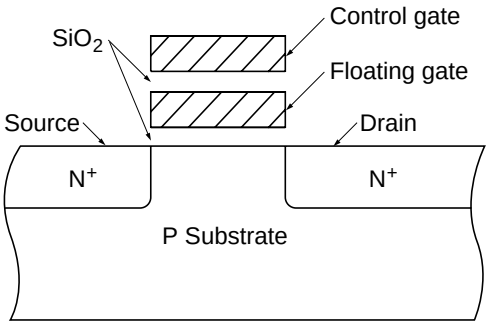


Figure 3-1 Cross Section of a EPROM Memory Cell

Figure 3-2 shows the fundamental characteristics of the EPROM transistor. While I_D in a non-programmed transistor begins to flow with V_G of about 1 V, the current in a programmed transistor does not flow until V_G rises to 7 to 10 V. Therefore, if the voltage of the word line applied to the control gate is about 5 V in the readout, a non-programmed memory transistor will be on, and the programmed memory transistor will be off. This means that the data can be read out by means of the same structure as a NOR-type mask ROM.

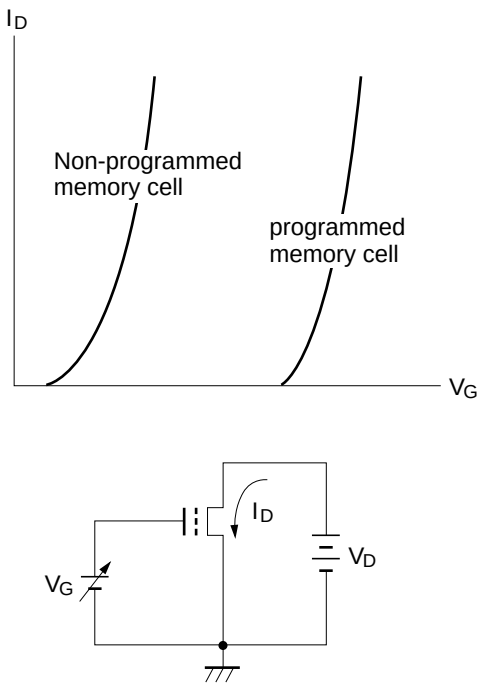


Figure 3-2 Fundamental Characteristics of a EPROM Memory Cell

Application

When shipped, all bits of the EPROM are at logic 1 with all electrons in the floating gate released (erased). Changing the logic 1 to logic 0, through the application of the specified waveform and voltage, programs the necessary information. The higher the V_{PP} voltage and the longer the program pulse width t_{PW}, the more electrons can be programmed in as shown in Figure 3-3. If V_{PP} exceeds the rated value, such as by overshoot, the pn junction of the memory may yield to permanent breakdown. To avoid this, check V_{PP} overshoot of the PROM programmer. Also, check negative-voltage-induced noise at other terminals, which can create a parasitic transistor effect and reduce the yield voltage. Hitachi's EPROMs can usually be written and erased more than 100 times.

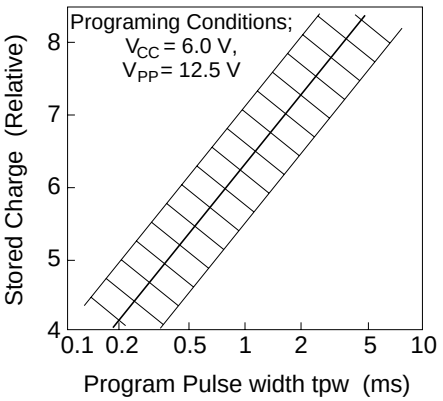


Figure 3-3 Standard Programming Characteristics of EPROMs

3.2 Erasing EPROM

EPROMs are erased by ultraviolet light exposure through a transparent window on the package. Electrons in the floating gate get energy from photons and become hot electrons again with enough energy to go over the energy barrier of SiO_2 film. The hot electrons go through to the control gate or the substrate and erasure is completed. Therefore, light with enough energy to get the electrons over the energy barrier of SiO_2 film is needed for erasure. Light energy is proportional to its frequency, and described as E = hv. E is the energy of light, h is Planck's constant, and v is light frequency. Erasure is not caused by light over certain wavelengths and under certain wavelengths. However, the erasure time depends upon the quantity of photons, therefore the erasure time cannot be shortened by using a shorter wavelength. Figure 3-4 shows the relation between wavelength and erasure effectiveness. Erasure starts at about 4000 Å and is saturated at about 3000 Å.

For erasure, the wavelength and minimum irradiation rate of ultraviolet light must be 2537 Å and 15 $W \cdot s/cm^2$ respectively. These conditions can be met by placing the device 2 to 3 cm below a 12,000 W/cm^2 UV lamp for about 20 minutes.

The UV transmittance of the transparent lid materials is about 70%. However, it is influenced by contamination or foreign materials on the lid surface. The contamination or foreign materials should be removed with a solvent that does not damage the package.

Figure 3-5 shows the EPROM standard erasure characteristics.

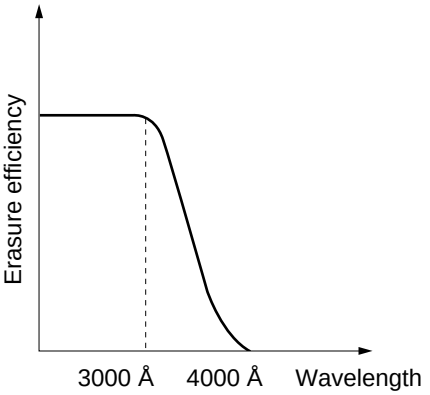


Figure 3-4 Erasure Efficiency of EPROM

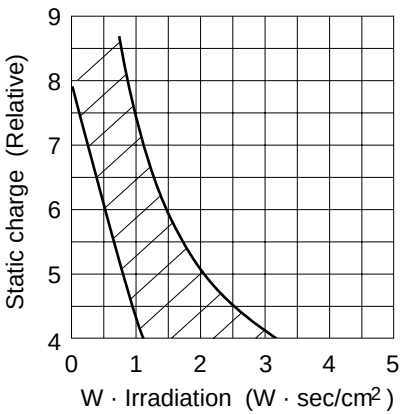


Figure 3-5 Standard Erasure Characteristics

3.3 EPROM Data Retention Characteristics

About 2 to 20 $\times$ 10^{-14} coulombs of electrons are accumulated in the floating gate when program-med. However, these electrons dissipate with time and the data may be inverted. The mechanism of electron dissipation is generally explained as follows.

Data Dissipation by Heat: The electrons at the floating gate are in a non-equilibrium state, so the dissipation of electrons by thermal energy is unavoidable. Therefore, the data retention time depends on temperature. Figure 3-6 shows typical data retention characteristics. The data retention time is proportional to the reciprocal of absolute temperature.

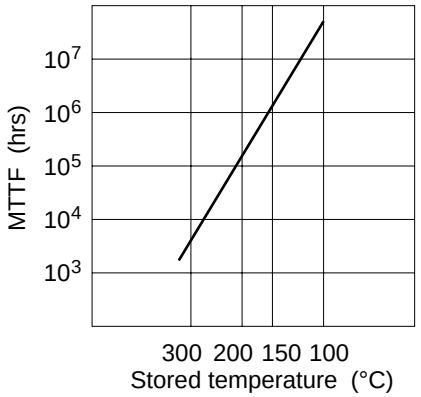


Figure 3-6 EPROM Data Retention Characteristics

Data Dissipation by Ultraviolet Light: Ultra-violet light at a wavelength no greater than 3000 to 4000 Å is capable of releasing the electric charge at the floating gate of the EPROM with varying efficiencies. Fluorescent light and sunlight contain some ultraviolet light, and so prolonged exposure to these lights can cause data corruption as a result of electric charge dissipation. Figure 3-7 shows the standard data retention time under an ultra-violet eraser, sunlight, and fluorescent lighting.

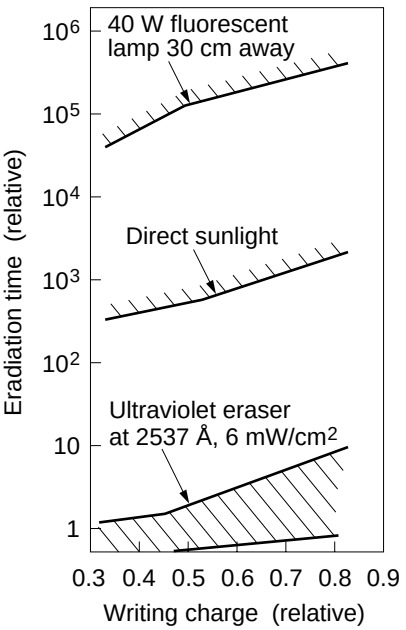


Figure 3-7 EPROM Data Retention Time

3.4 Optimized High Speed Programming

With the increase of EPROM density, the time for programming becomes more important. Methods for high speed programming have been developed and put into practical use for each EPROM generation.

There are three methods for high speed pro-gramming.

Figure 3-8 shows the relative programming times of these methods.

Please refer to the data sheet about each programming method.

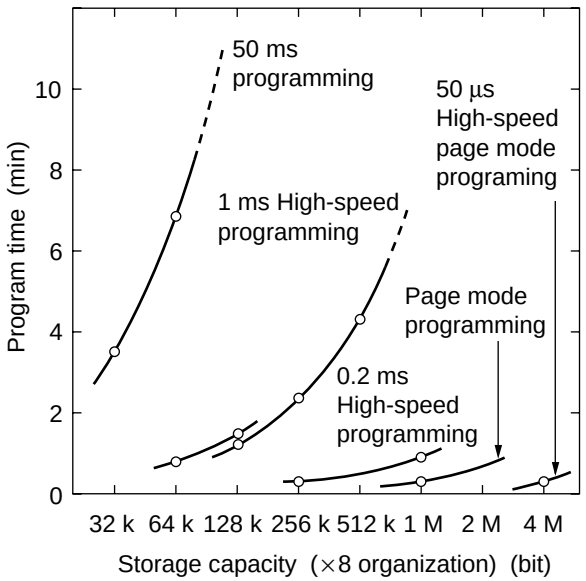


Figure 3-8 Comparison of Shortened Programming Time

3.5 Device Identifier Code

EPROM programming conditions depend on the EPROM manufacturers' standards and specific device types. Confusion on the proper use of varying methods required may cause poor or failing operation. As a countermeasure, some EPROMs provide embedded device identifier codes including such information as the manu-facturer and device type. Some newly developed commercial EPROM programmers can set write conditions automatically by recognizing this code.

Different programming conditions are as follows.

1. Program voltage
2. Program timing
3. High performance programming algorithm
4. Pin configuration

Application

The Hitachi EPROM has a device identifier code area adjacent to the memory access area as shown in Figure 3-9.

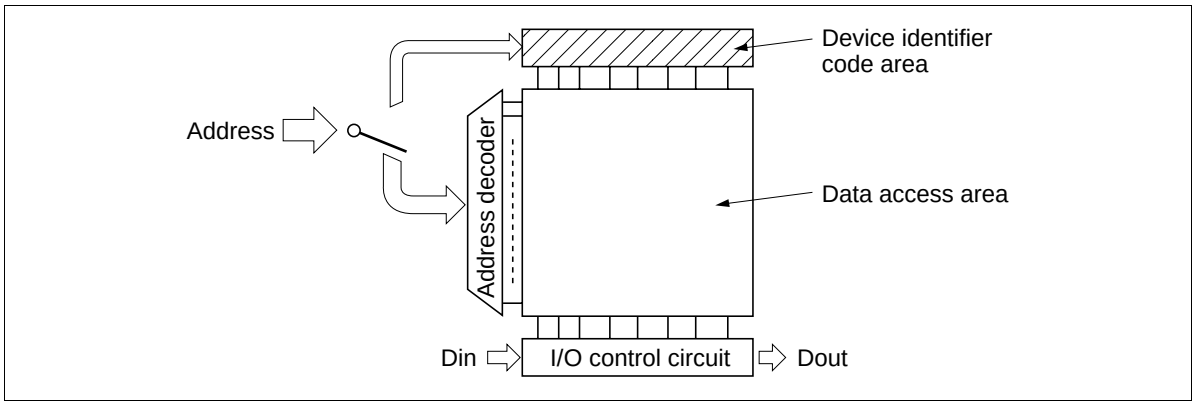


Figure 3-9 Device Identifier Code

Table 3-1 describes how to use the device identifier code. Setting A9 at 12 V and A1-A8 and A10-A13 at V_{IL}, access the device identifier code area and I/O0-I/O7, and output the programming condition code with V_{IL} or V_{IH} of A0.

Table 3-1 Hitachi EPROM Device Identifier Code

		A_0	I/O8-I/O15	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Hex Data
Manufac-turer code	Hitachi	V_{IL}	—	0	0	0	0	0	1	1	1	07
ROM code	HN27C256H	V_{IH}	—	0	0	1	1	0	0	0	1	31
	HN27C256A	V_{IH}	—	0	0	1	1	0	0	0	1	31
	HN27C1024H	V_{IH}	—	1	0	1	1	1	0	1	0	BA
	HN27C101A	V_{IH}	—	0	0	1	1	1	0	0	0	38
	HN27V101A	V_{IH}	—	0	0	1	1	1	0	0	0	38
	HN27C301A	V_{IH}	—	1	0	1	1	1	0	0	1	B9
	HN27C4096	V_{IH}	—	1	0	1	0	0	0	1	0	A2
	HN27C4001	V_{IH}	—	0	0	1	0	0	0	0	0	20
	HN27C4096A	V_{IH}	—	1	0	1	0	0	0	1	0	A2
	HN27C4000	V_{IH}	—	1	0	1	0	0	0	0	1	A1
	HN27C4096H	V_{IH}	—	1	0	1	0	0	0	1	0	A2

A9: 12 V

A1-A8, A10-A13: V_{IL}

A14, A15: H or L

3.6 Shielding Label

When using an EPROM in an environment where it can be exposed to ultraviolet light, Hitachi recommends placing a shielding label over the transparent lid to absorb the ultraviolet light. In choosing a shielding label, the following points should be carefully checked.

1. Adhesiveness (mechanical strength)

   Avoid repeated removal and reattachments, or exposure to dust that may reduce the adhesive strength. Ultraviolet erasure and reprogram-ming are recommended after stripping off an attached label. (When the need arises to change a label, it is advisable to place a new one over the old one since peeling may create a static charge.)
2. Allowable temperature range

   Use the shielding label in an environment where temperature is stable within the specified allowable temperature range. Beyond the specified temperature range, the paste on the label may harden or stick too tightly. When it hardens, the label may come off easily. When it sticks too tightly, the paste may remain on the window glass after the label has been removed.
3. Moisture resistance

   Use the shielding label in an environment where humidity is stable within the specified allowable humidity range.

3.7 EPROM Programmer

The EPROM programmer stores the user's program in its internal RAM and writes the program in the EPROM. For this programming, at least three functions are necessary: the blank check function prior to programming, programming function, and verify function after programming. Figure 3-10 shows the programming flowchart. Some programmers check for pin contact failure or reverse insertion before the blank check.

The outline of each check is as follows.

1. Pin contact check

   In the ROM pin and socket connection test, checking is normally performed by detecting forward current at each EPROM pin. Care is necessary as this forward biased resistance differs in products of each company.
2. Reverse insertion check

   This check detects the reverse insertion of the device, then places the equipment in reset mode and protects the device and equipment if the condition is found.
3. Blank check

   This check is performed before programming. It checks whether the device is an erased EPROM, or it prevents EPROM reprogram-ming. Since output data in the erased condi-tion is high, the check is for whether the data in the EPROM are all 1s. It will fail even if one bit is 0. Normally, it is designed to provide a warning with a lamp or buzzer.

4. Programming

   The function of programming the data from the internal RAM of the programmer into the EPROM will fail when programming cannot be done. The normal flow is as shown in Figure 3-11. The EPROM data for a target location will be read out prior to programming and compared with the programming data intended for that location. If the data matches, programming will be skipped. If they differ, programming will be performed. Then, the data will be read back and compared with the original programming data, and if they match, the programmer will progress to the next address.

5. Verify

   This function checks after programming completion whether or not the programming is correct when comparing with the data in the internal RAM of the programmer. It will fail when they do not match. Normally, when it fails, it lights the fail lamp and displays the address and data.

6. How to input a program

   Table 3-2 shows several methods for inputting the program data to the internal RAM of the programmer. Normally, paper tape input and teletypewriter input are preferred options.

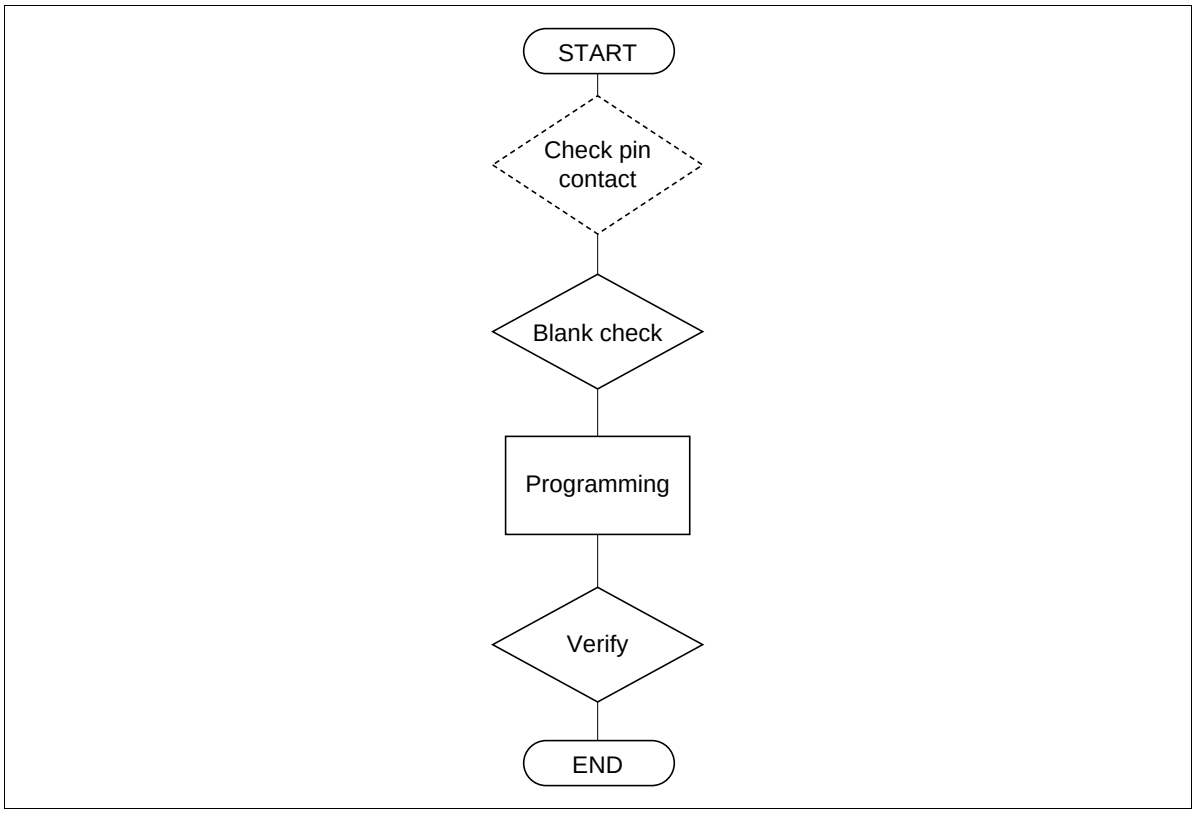


Figure 3-10 Programming Flowchart of EPROM Programmer (1)

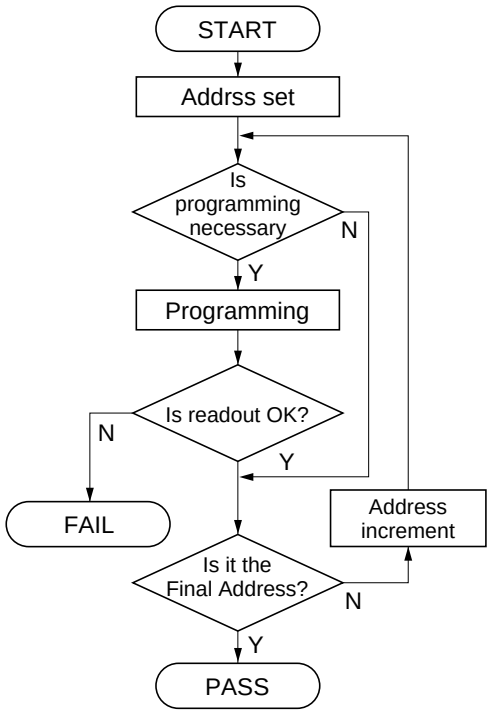


Figure 3-11 Programming Flowchart of EPROM Programmer (2)

Table 3-2 EPROM Data Input

Method	Content
Copy input	Input by copying the master ROM.
Manual input	Input by the keyswitches on the front panel. Used for correction or revision of programs.
Paper tape input	Paper tape furnished from the host system is read with the tape reader.
Teletypewriter input	Input with the teletypewiter. Preparation, correction, and list preparation of the program can be made.

3.8 Handling EPROMs

If touched by a charged human body or rubbed with plastics or dry cloth, the glass window of an EPROM generates static electricity which causes device malfunctions. Typical malfunctions are faulty blanking and write margin setting that give the false impression that information has been correctly written in. As already reported at international conferences concerning the reliability of LSI chips, this is due to the prolonged retention of electric charge (resulting from static electricity) on the glass window. Such malfunctions can be eliminated by neutralizing the charges by irradiating the EPROM with ultraviolet rays for a short time. The EPROM should be reprogrammed after this irradiation since it also reduces the electric charges in the floating gates. The basic countermeasure is to prevent the charging of the window, which can be achieved by the following methods, as in the prevention of common static breakdown of ICs.

1. Ground operators who handle the EPROM.
   Avoid using things such as gloves that may generate static electricity.
2. Avoid rubbing the glass window with plastic or other materials that may generate static electricity.
3. Avoid the use of coolant sprays which may contain some free ions.
4. Use shielding labels (especially those containing conductive substances) that can evenly distribute any established charge.

3.9 Ensuring OTPROM Reliability

The one-time-programmable ROM (OTPROM) has two forms: standard dual in-line package (DIP) and small outline package (SOP). It is only one-time programmable because it has no window for ultraviolet light exposure; testing by programming and erasure cannot be performed after it is assembled.

As a means of improving reliability, Hitachi performs screening tests for programming, access time, and data retention on OTPROM wafers during the manufacturing process.

However, rare defects may occur in the assembly process that cannot be completely removed in the final test screening which is only a reading test. Therefore, Hitachi recommends that users perform high temperature baking after programming these devices to ensure the highest reliability.

Detailed conditions and procedures for screening are shown in Figure 3-12. First, program and verify the devices. Then leave them without bias at 125 to 150°C for 24 to 48 hours.

After that, check the readout function, and discard chips with data retention failures.

From the results of devices in which the recommended screening test is properly performed, we find the data retention character-istics of OTPROMs are generally equal to EPROMs.

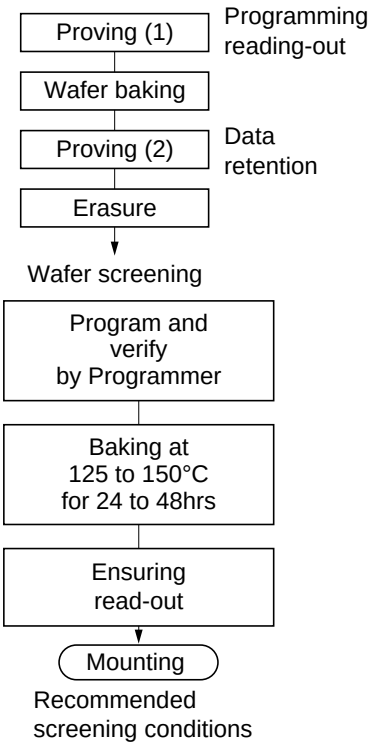


Figure 3-12 Screening Flowchart of OTPROM

4. Mask ROM Programming Instruction

The writing of custom program code into mask ROMs is performed by a CAD system on a large-scale computer. ROM code data should conform to the specifications given below, using either EPROM or floppy disk. Additional instructions, such as chip select or customer part numbers, should be noted on the "ROM Specification Identification Sheet."

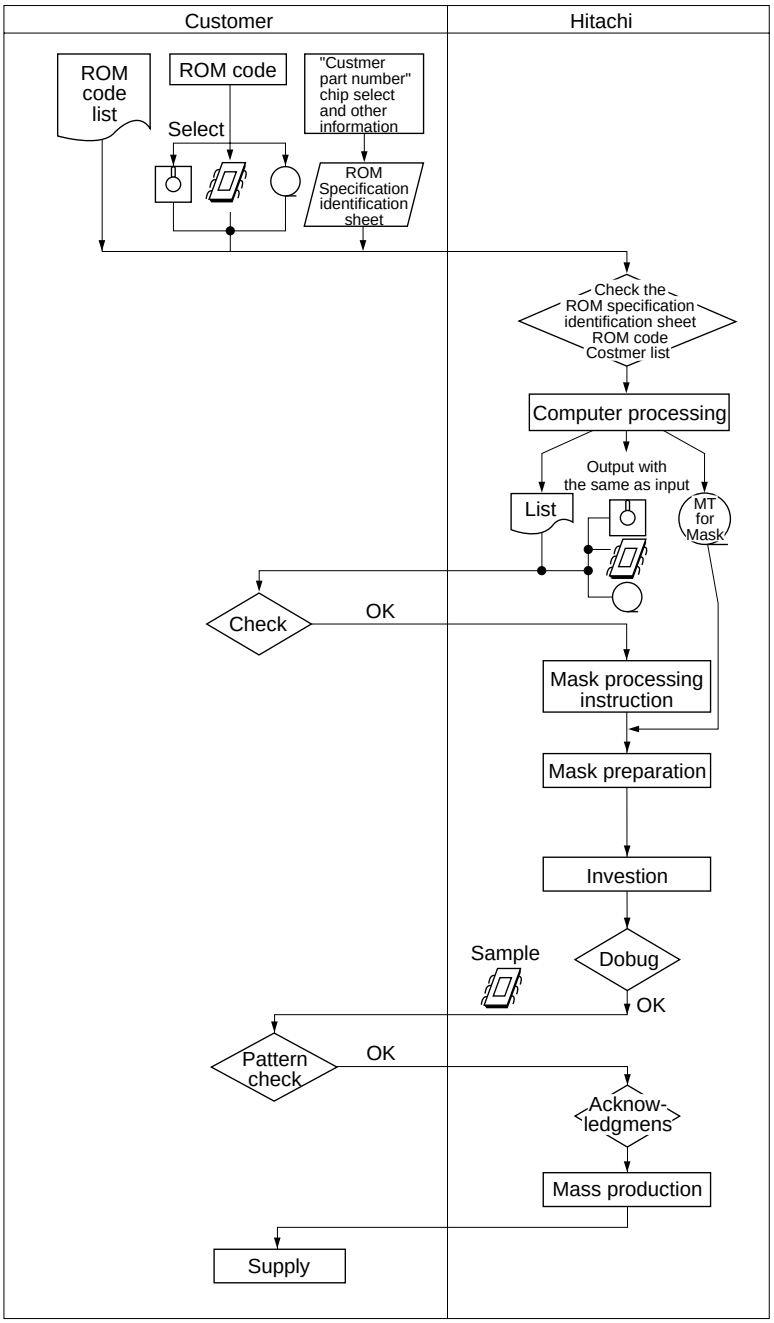


Figure 4-1 Mask ROM Development Flowchart

5. Instructions for Using Memory Devices

5.1 Prevention of Electrostatic Discharge

As semiconductor memory designs are based on a very fine pattern, they can be subject to malfunction or defects caused by static electricity. Though the built-in protection circuits assure unaffected reliability in normal use, devices should be handled with these precautions:

1. In transporting and storing memory devices, place them in a conductive magazine or wrapper, or put all pins of each device into a conductive mat, so that they are kept at the same potential. Manufacturers should give sufficient consideration on proper packing when shipping their products.
2. When the devices are to be touched during mounting or inspection, the handler must be grounded. Do not forget to connect a resistor (1 MΩ approximately is desirable) in series for protect 10 n against electrical shock.
3. Keep the relative ambient humidity at about 50% during processing.
4. For working clothes, cotton is preferable to synthetic fabrics.
5. Use a soldering iron operating at low voltage (12 V or 24 V, if possible) with its tip grounded.
6. When transporting a board with memory devices mounted on it, enclose it with conductive materials.
7. Use conductive materials of high resistance (about 109 ohms) to protect the devices from electrostatic discharge. Otherwise, if accident-ally put in contact with conductive materials such as a metal sheet, the devices may deteriorate or even breakdown, owing to the sudden release of charge stored on the surface.
8. Never set a system in which memory devices are used near anything that generates high voltage (e.g., a CRT anode electrode, etc.).

5.2 Using CMOS Memories

As shown in Figure 5-1, the input of a CMOS memory is connected to the gate of an inverter consisting of PMOS and NMOS transistors. Figure 5-2 shows the relationship between the input voltage and current within the inverter. The top and bottom transistors turn on and create a current flow when the input voltage reaches an intermediate level. Therefore it is necessary to keep the input voltage below 0.2 V or above V_{CC} - 0.2 V in order to minimize power consumption. The data sheet specifies the standby current for two cases of input level (with minimum V_{IH} and maximum V_{IL}, and with 0.2 V or V_{CC} - 0.2 V), and the difference in values as being remarkably great. Some memory devices are designed to cut off such current flow in the standby mode by the control of input signals, but this depends on the specific device type. This should be confirmed in data sheets for each device type.

Application

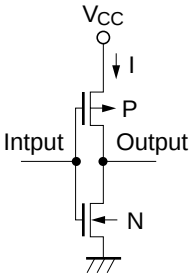


Figure 5-1 CMOS Inverter

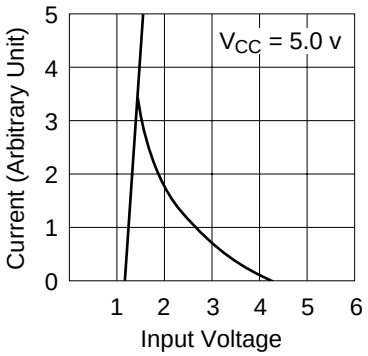


Figure 5-2 Relationship Between Input Voltage and Current in a CMOS Inverter

Another problem peculiar to CMOS devices is latch up. Figure 5-3 shows the cross section of a CMOS inverter and the structure of a parasitic bipolar transistor. The equivalent circuit of the parasitic thyristor is shown in Figure 5-4. When positive DC current or pulse noise is applied (Figure 5-4a), T_{R3} is turned on owing to the bias voltage generated between the base and emitter. Also, trigger current flows to ground through R_P, the base resistance of T_{R2}. As a result, T_{R2} becomes conductive and the current flows from power supply (V_{CC}) through the base resistance of TR1 (R_N), which also puts T_{R1} into conduction. Then as the base of T_{R2} is rebiased by the collector current from T_{R1}, the closed loop consisting of T_{R1} and T_{R2} reacts. Thus, current flows constantly between the power supply (V_{CC}) and ground even without the trigger current caused by outside noise.

Latch up can also be caused by a negative pulse (Figure 5-4b). Most semiconductor memory manufacturers are trying to improve latch up immunity in their products. Hitachi provides a broad enough guard band by applying a diffusion layer around the inputs and outputs, taking care not to connect the input to the p^+ diffusion layer. The input voltage for the 64-kbit static RAM HM62256, for example, is specified as follows:

V_{IH} max 6.0 V (not dependent on V_{CC})
V_{IL} min 3.0 V (pulse width = 50 ns)
-0.5 V (DC level)

Thus almost no consideration for latch up is required in system designs using these devices.

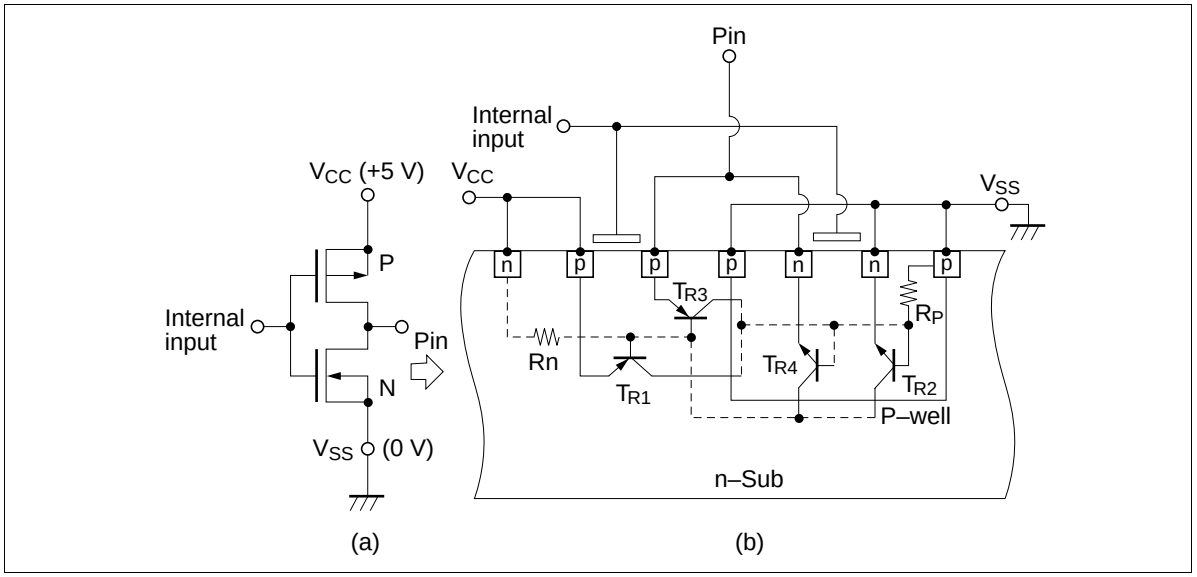


Figure 5-3 Cross Section Structure of CMOS Inverter

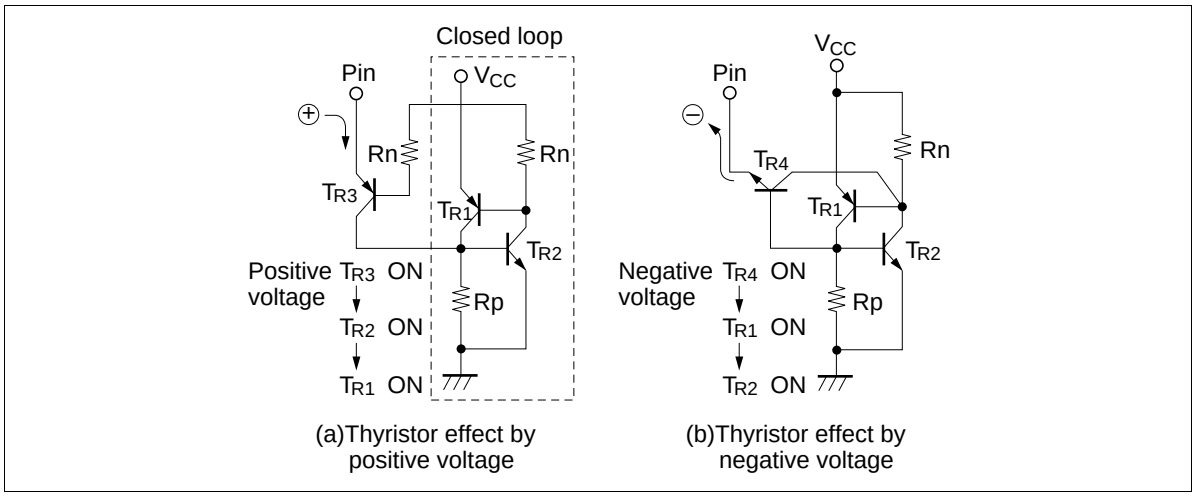


Figure 5-4 Equivalent Circuit of Parasitic Thyristor

5.3 Noise Prevention

Noise in semiconductor memories is roughly classified as input signal noise and power supply noise.

Input Signal Noise: Input signal noise is caused by overshoot and undershoot. If either of them exceeds the recommended DC operating conditions, normal operation is hindered, and a voltage over the absolute maximum rating will break the device. When operating high speed systems, special care is required to prevent input signal noise.

Application

The noise can be prevented by inserting a serial resistance of less than 50 ohms into each input or a terminating resistance into the input line. Actually, however, input signal noise can be simply reduced by a stable power supply line, because the noise is often caused by an unstable reference voltage (ground level).

Power Supply Noise: Power supply noise can be classed as low-frequency and high-frequency as shown in Figure 5-5. To assure a stable memory operation, combined low- and high-frequency noise should be held below 10 percent of the standard level of the peak-to-peak power supply voltage.

Devices like dynamic RAMs, which operate from clock signals, or high speed CMOS static RAMs, through which current flows during the transition of signals, consume high peak current. When a power supply does not have enough capacity for the peak current, the voltage drops. And if the recovery rate of the power supply synchronizes with its time constant, it may start oscillating. To reduce the influence of the peak current, a bypass capacitor of 0.1-0.01 μF should be inserted near the device. The following points must be considered in designing the layout of a board:

1. For bypass capacitors, use titanium, ceramic, or tantalum capacitors which have better high-frequency characteristics.
2. Bypass capacitors must be applied to the power supply pins of memory devices as near as possible, and inductance in the path from the V_{CC} pin to V_{SS} pin through the bypass capacitor must be kept as low as possible.
3. The line connected to the power supply on the board should be as wide as possible.
4. It is preferable for the power supply line to be at right angles to devices selected at the same time, otherwise too much peak current will flow through one power supply line at a time.

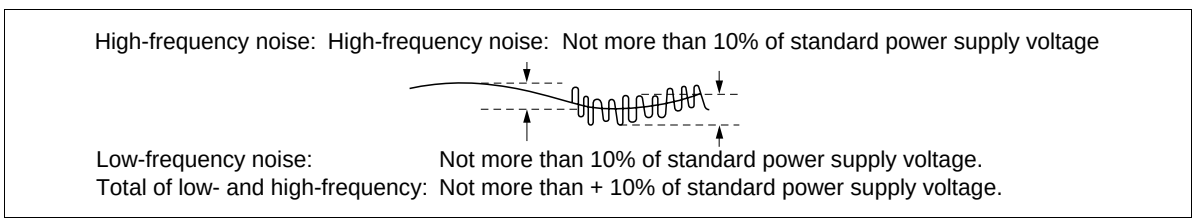


Figure 5-5 Power Supply Noise

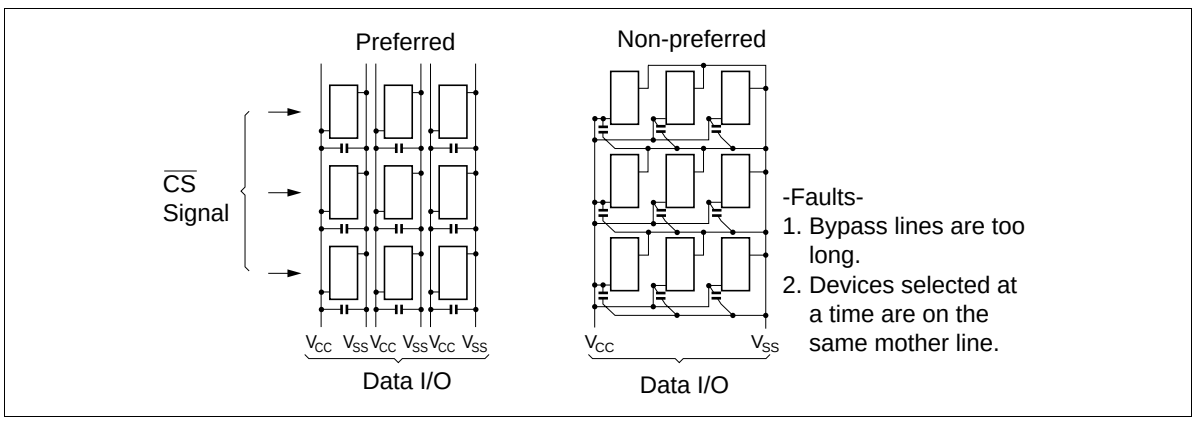


Figure 5-6 Examples of a Power Supply Board Pattern